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US DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEYS DOCKET NUMBER: P02,0022

U.S.APPLICATION NO. (if known, see 37 CFR 1.5): 10/048207

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/DE99/02339	29 July 1999	29 July 1999

TITLE OF INVENTION: "METHOD FOR PRODUCING INTEGRATED SEMICONDUCTOR COMPONENTS"

APPLICANT(S) FOR DO/EO/US: Lars-Peter Heineck, Tobias Jacobs and Josef Winnerl

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☒ This express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay.
4. ☒ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.
5. ☒ A copy of International Application as filed (35 U.S.C. 371(c)(2))
   a. ☒ is transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ has been transmitted by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US)
6. ☒ A translation of the International Application into English (35 U.S.C. 371(c)(2).
7. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. §371(c)(3))
   a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ have been transmitted by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☒ have not been made and will not be made.
8. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)). **(Three Separate Executed Declarations)**
10. ☒ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11. to 16. below concern other document(s) or information included:

11. ☒ An Information Disclosure Statement under 37 C.F.R. 1.97 and 1.98; **(PTO 1449, Prior Art, Search Report)**.
12. ☒ An assignment document for recording. A separate cover sheet in compliance with 37 C.F.R. 3.28 and 3.31 is included. **(Three Separate Executed Assignments)**
    (See Attached Envelope)
13. ☒ A FIRST preliminary amendment.
    ☐ A SECOND or SUBSEQUENT preliminary amendment.
14. ☒ A substitute specification.
15. ☐ A change of power of attorney and/or address letter.
16. ☒ Other items or information:
    a. ☒ Submission of Drawings - 9 sheets
    b. ☒ Submission of Proposed Drawing Changes
    c. ☒ EXPRESS MAIL #EL843746043US dated January 28, 2002

JC13 Rec'd PCT/PTO 28 JAN 2002

U.S.APPLICATION NO. (if known, see 37 C.F.R. 1.5)	INTERNATIONAL APPLICATION NO.	ATTORNEY'S DOCKET NUMBER
10/048207	PCT/DE99/02339	P02,0022

17. ☒ The following fees are submitted:	CALCULATIONS	PTO USE ONLY
BASIC NATIONAL FEE (37 C.F.R. 1.492(a)(1)-(5):		
Search Report has been prepared by the EPO or JPO $890.00		
International preliminary examination fee paid to USPTO (37 C.F.R. 1.482) . . . $670.00		
No international preliminary examination fee paid to USPTO (37 C.F.R. 1.482) but international search fee paid to USPTO (37 C.F.R. 1.445(a)(2) $760.00		
Neither international preliminary examination fee (37 C.F.R. 1.482) nor international search fee (37 C.F.R. 1.445(a)(2) paid to USPTO $970.00		
International preliminary examination fee paid to USPTO (37 C.F.R. 1.482) and all claims satisfied provisions of PCT Article 33(2)-(4) . . . . . $ 96.00		
ENTER APPROPRIATE BASIC FEE AMOUNT =	$ 890.00	
Surcharge of $130.00 for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 C.F.R. 1.492(e)).	$	

Claims	Number Filed		Number Extra	Rate		
Total Claims	10	- 20 =	0	X $18.00	$	
Independent Claims	1	- 3 =	0	X $84.00	$	
Multiple Dependent Claims				$280.00 +	$	
				TOTAL OF ABOVE CALCULATIONS =	$ 890.00	
Reduction by 1/2 for filing by small entity, if applicable. Verified Small Entity statement must also be filed. (Note 37 C.F.R. 1.9, 1.27, 1.28)					$	
				SUBTOTAL =	$ 890.00	
Processing fee of $130.00 for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(f)). +					$	
				TOTAL NATIONAL FEE =	$ 890.00	
Fee for recording the enclosed assignment (37 C.F.R. 1.21(h). The assignment must be accompanied by an appropriate cover sheet (37 C.F.R. 3.28, 3.31). $40.00 per property +					**SEE ATTACHED ENVELOPE**	
				TOTAL FEES ENCLOSED =	$ 890.00	
				Amount to be refunded	$	
				charged	$	

a. ☒ A check in the amount of $890.00 to cover the above fees is enclosed.

b. ☐ Please charge my Deposit Account No. _____ in the amount of $ _____ to cover the above fees. A duplicate copy of this sheet is enclosed.

c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. **501519**. A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 C.F.R. 1.494 or 1.495 has not been met, a petition to revive (37 C.F.R. 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

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**IN THE UNITED STATES ELECTED OFFICE OF
THE UNITED STATES PATENT AND TRADEMARK OFFICE
UNDER THE PATENT COOPERATION TREATY - CHAPTER II**

PRELIMINARY AMENDMENT

APPLICANTS: Lars-Peter Heineck, Tobias Jacobs and Josef Winnerl

ATTORNEY DOCKET NO.: P02,0022

SERIAL NO.: EXAMINER:

FILING DATE: ART UNIT:

INTERNATIONAL APPLICATION NO.: PCT/DE99/02339

INTERNATIONAL FILING DATE: 29 July 1999

INVENTION: "METHOD FOR PRODUCING INTEGRATED SEMICONDUCTOR COMPONENTS"

BOX PCT
Assistant Commissioner for Patents
Washington, D.C. 20231

S I R:

Please amend the above-identified International Application before entry into the National Stage before the U.S. Patent and Trademark Office under 35 USC 371 as follows:

IN THE SPECIFICATION:

Please replace original pages 1-15 and substitute page 16 with the attached Substitute Specification.

IN THE ABSTRACT:

Please replace the Abstract with the attached unnumbered page entitled ABSTRACT OF THE DISCLOSURE".

IN THE CLAIMS:

Please cancel claims 1-8 on substitute pages 16 and 17, without prejudice, and add the following claims:

--9. A method for producing an integrated semiconductor component comprising the steps of preparing a semiconductor substrate having at least one first region and at least one second region; producing gate paths in the first region and the second region of the semiconductor substrate; producing source/drain regions neighboring the gate paths in the first region of the semiconductor substrate; forming at least two spacers on gate paths in the first region; producing source/drain regions neighboring the gate paths in the second region of the semiconductor substrate; forming sacrificial contacts in the second region before all spacers are formed in the first region; and preparing contacts to predetermined source/drain regions in the second region and the first region.--

--10. A method according to claim 9, wherein the spacers are formed of a material selected from a group consisting of silicon oxide, silicon nitride and oxynitride.--

--11. A method according to claim 9, wherein the step of producing gate paths includes applying a polysilicon layer on the semiconductor substrate, providing a protective layer selected from a group consisting of silicon nitride, silicon oxide

and oxynitride layers on the polysilicon layer and then structuring the polysilicon layer and protective layer to form the gate path.--

--12. A method according to claim 11, wherein the protective layer is formed with a thickness so that the protective layer exhibits a thickness of less than 100nm after the structuring step.--

--13. A method according to claim 11, which includes, after the step of forming sacrificial contacts and prior to the step of preparing contacts to the predetermined source/drain regions, removing the protective layer from the gate paths, at least in the first region, and then doping the gate paths in the first region with a dopant having different conductive types.--

--14. A method according to claim 13, which includes, after the step of doping the gate paths in the first region, generating a silicide layer on the doped gate paths of the first region of the semiconductor substrate.--

--15. A method according to claim 14, wherein the silicide layer is selected from silicides consisting of $CoSi_2$, $TaSi_2$, $TiSi_2$ and WSi_x.--

--16. A method according to claim 15, wherein the step of generating a silicide comprises the step of providing a metal selected from Co, Ta, Ti and W on the gate paths of the first region and subsequently heating to convert the metal into a metal silicide layer.--

--17. A method according to claim 14, wherein the step of generating a silicide layer on the gate paths of the first region includes applying a metal capable of forming a silicide onto the gate paths of the first region and subsequently heating to create the silicide layer.--

--18. A method according to claim 9, which includes, prior to the step of forming contacts to the predetermined source/drain region of the second region, generating silicide layers on the gate paths of the first region of the semiconductor substrate.--

REMARKS

Claims 9-18 are presented for examination.

By this amendment, the translation of the PCT Application has been amended to correct typographical and grammatical errors therein and to add headings, which changes are included in the attached Substitute Specification, which replaces the original pages 1-15 and substitute page 16 of the translation. A marked-up version showing the amendments is also attached. An Abstract of the Disclosure has been added on the attached unnumbered page. Claims 1-8 on substitute pages 16 and 17 have been cancelled and claims 9-19, which have been drafted to place them in form for examination in the United States Patent Office and to remove multiple-dependency have been added.

Respectfully submitted,

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ABSTRACT OF THE DISCLOSURE

To enable increasing the integration density of a semiconductor component, for example a memory cell field, gate paths or tracks are formed on a first and a second region of the semiconductor substrate along with source/drain regions adjacent these gate paths. Then, contacts for the source/drain regions in the second area are formed followed by forming spacers on the gate paths or tracks.

Appendix 9/pgs

TITLE

METHOD FOR PRODUCING INTEGRATED SEMICONDUCTOR COMPONENTS

BACKGROUND of THE INVENTION

The present invention is directed to a method for producing an integrated semiconductor component. In particular, the present invention is directed to a method for producing ~~and~~ either an integrated DRAM ~~or~~, an embedded DRAM or, respectively, an embedded SRAM semiconductor component.

The goal of many developments in microelectronics is to constantly lower the costs to be expended for the realization of a specific electronic function and, thus, to constantly increase the productivity. The guarantee for increasing productivity in recent years was and is, thereby, the constant structural miniaturization of the semiconductor components. In particular, field effect transistors are being constantly miniaturized and arranged in integrated circuits having the highest packing density.

In order to carry out their function, field effect transistors must be connected to other field effect transistors and to the outside world. To that end, contacts to the diffusion regions of the transistors must be produced. In methods for manufacturing logic circuits, for example, via holes to the diffusion regions of the transistors are produced by a photo technique and an etching. Since this formation of the via holes is usually not implemented to be self-aligned, an adequately large safety margin between the gate track and the via hole must be ~~adhered to~~ provided and this margin, of course, has a negative influence on the integration density.

In methods for producing DRAM semiconductor components, self-aligned contacts are usually produced. Via holes are thereby usually etched in a BPSG layer deposited between the gate paths. Subsequently, these via holes are filled with a conductive material, so that a conductive connection is created.

The production of these via holes, however, becomes more and more difficult with ongoing structural miniaturization. In modern field effect transistors, a number of spacers are produced at the sidewalls of the gate webs, these, in interaction with suitable dopant implantations, ~~seeing~~ see to it that the dopant profiles suitable for the respective purpose can be produced in the source/drain regions. Due to the spacers arranged between the gate paths and the demand that the via hole should be arranged

between the spacers insofar as possible, the distance between the gate paths or, respectively, the diffusion region that serves the purpose of contacting must be selected adequately large, and this ~~having~~ has a negative influence on the integration density that can be achieved.

When etching the via holes, the gate paths dare not be damaged, since a short would otherwise arise between the diffusion contact and the gate. Since, despite all efforts, one cannot prevent the gate paths from being attacked when etching the via holes, a thick protective layer, which was referred to as a "cap", is usually arranged on the gate paths, and this ~~being~~ is intended to prevent a short between contact and gate. The relatively great thickness of this protective layer, however, deteriorates the quality of the gate paths and usually prevents a silicidization of the gate paths as well as the subsequent doping of the polysilicon of the gate paths (dual work function gate).

Due to the tight conditions between the gate paths, it is necessary that the insulation layer be subjected to a temperature treatment at relatively high temperatures in order to achieve a flowing of the insulation layer. Nonetheless, holes, what are referred to as voids, can occur between the gate paths ~~in~~ during the deposition of the insulation layer. When the via holes are then formed, it can occur that two via holes are connected to one another via a void. In the subsequent filling of the via holes with a conductive material, the voids are usually also filled, so that a short between two contacts can arise that which possibly leads to the outage of the entire circuit.

SUMMARY OF THE INVENTION

It is therefore the object of the present invention to offer a method for producing an integrated semiconductor component that minimizes or, respectively, entirely avoids said these problems.

~~This object is inventively achieved by the methods for producing an integrated semiconductor component according to independent patent claims 1 or 3. Further advantageous embodiments, properties and aspects of the present invention derive from the dependent claims, from the specification and from the attached drawings.~~

Inventively, a method for producing an integrated semiconductor component is offered that comprises the following steps:

a) preparing a semiconductor substrate having at least one first region and at least one second region ~~is prepared~~;

b) producing gate paths ~~are produced~~ in the first and ~~in~~ the second ~~region~~ regions of the semiconductor substrate;

c) producing source/drain regions neighboring the gate paths and at least two spacers at the gate paths ~~are produced~~ in the first region of the semiconductor substrate;

d) producing source/drain regions ~~are produced~~ neighboring the gate paths in the second region of the semiconductor substrate, and forming contacts to predetermined source/drain regions ~~are formed~~ before all spacers have been produced in the first region of the semiconductor substrate.

Inventively, a method for producing an integrated semiconductor component ~~having the following steps~~ is also offered and has the following steps.

a) preparing a semiconductor substrate having at least one first region and at least one second region ~~is prepared~~;

b) producing gate paths ~~are produced~~ in the first and ~~in~~ the second ~~region~~ regions of the semiconductor substrate;

c) producing source/drain regions neighboring the gate paths as well as at least two spaces at the gate paths ~~are produced~~ in the first region of the semiconductor substrate;

d) producing source/drain regions neighboring the gate paths ~~are produced~~ in the second region of the semiconductor substrate; and pre-doping contacts to predetermined source/drain regions ~~are prepared~~ before all spacers in the first region of the semiconductor substrate have been produced.

The inventive methods have the advantage that integration density in the second region of the semiconductor substrate can be noticeably increased. As a result of the feature that the formation of the contacts to the source/drain regions is undertaken or, respectively, readied in the second region of the semiconductor substrate at a time at which all spacers have not yet been produced, no unnecessary

spacer production occurs in the second region, ~~as a result whereof~~ chip area ~~can be saved~~. The saved area can, for example, be used in order to arrange the gate paths closer together in the second region. The spacers can thereby be employed as an aid for setting the desired dopant profiles and/or as lateral insulation of the gate paths.

~~Further~~, the inventive methods can be integrated without difficulty in a process sequence that already exists for producing a semiconductor component. In particular, the process steps for the manufacture of very fast logic circuits can be retained nearly unmodified. Problems ~~such as derive at~~ traditional methods due to the occurrence of voids between the transistors can be clearly reduced or, ~~respectively,~~ entirely avoided given the inventive methods. Due to the early formation or, respectively, preparation of the contacts, high aspect ratios can be avoided, as a result ~~whereof~~, the processes can be implemented more stably overall. The contacts can thereby also already ~~be~~ formed or, respectively, prepared at a time at which the source/drain regions have not yet been formed ~~at all~~.

According to a preferred embodiment, landing pads are formed in the second region of the semiconductor substrate for preparing the contacts to predetermined source/drain regions. Doped polysilicon is preferably employed for forming the landing pads or, respectively, the contacts themselves.

According to another preferred embodiment, sacrificial contacts are formed in the second region of the semiconductor substrate for preparing the contacts to predetermined source/drain regions. The sacrificial contacts likewise prevent the production of unnecessary spacers ~~at~~ the gate paths in the second region of the semiconductor substrate. They are removed only when the actual contacts to the source/drain regions are formed.

According to a preferred embodiment, the spacers are formed of silicon oxide, silicon nitride or oxynitride. To that end, a silicon oxide layer, silicon nitride layer or oxynitride layer is deposited over the gate paths and etched back with an anisotropic etching, so that parts of these layers remain at the sidewalls of the gate paths. By employing these spacers, the dopings of the source/drain region can be set very precisely ~~corresponding~~ to the respective demands.

According to another preferred embodiment, the gate paths are formed in ~~that~~ a polysilicon layer and a protective layer, particularly a silicon nitride layer, silicon oxide layer or oxynitride layer is produced and these layers are structured in common to form gate paths. It is thereby particularly preferred when the protective layer is produced with a thickness ~~such~~ so that the protective layer comprises a thickness less than 100 nm, preferably in a range between 40 and 60 nm, after the gate structuring. This protective layer is frequently referred to as a "cap" and, in traditional processes, serves among other things as a hard mask for gate structuring and for protecting the gate paths during an etching process for producing the via holes. In the prior art, a dry-etching process that etches oxide selectively relative to the cap material must be utilized for this purpose. Since the structure to be etched exhibits a high aspect ratio in the prior art, the selectivity of the etching process is not very high, and a relatively thick "cap" must be employed in order to avoid a short between the gate path and the contact.

Since the formation of the contact is already undertaken or, respectively, prepared at a very early stage ~~given~~ in the inventive methods, the "cap" now serves only for insulating the gate path from the contact and can therefore be selected relatively thin. Accordingly, the "cap" can be completely removed from the gate paths in the first region in later process steps, for example when etching a nitride spacer, and without additional process steps, this ~~opening~~ opens up the possibility of doping various gate paths with different dopants and thus constructing what are referred to as dual work function gates. ~~Further~~ In addition, the gate paths can be silicided in this way, and as a result of the silicidation, ~~whereof~~ the resistance of the gate paths is clearly reduced.

It is also preferred when the gate paths in the first region of the semiconductor substrate are doped with dopants having different conductivity types. As a result of what is referred to as these dual work function gates, extremely high-performance logic circuits can be constructed. In this way, the supply voltage can also be reduced without incurring any losses in the switching speed.

For reducing the resistances of the gate paths, it is preferred when silicide layers are produced on the gate paths in the first region of the semiconductor substrate. In particular, it is preferred when $CoSi_2$, $TaSi_2$, $TiSi_2$ or WSi_x is employed as silicide layers, and these silicide layers are produced by a salicide method.

The invention is explained in greater detail below with reference to the drawings. ~~Shown are:~~ Brief Description of the Drawing,

Figs. 1 - 8 are cross-sectional views illustrating various steps of a method according to a first exemplary embodiment of the present invention;

Figs. 9 - 12 are cross-sectional views illustrating various steps of a method according to a second exemplary embodiment of the present invention; and

Figs. 13-18 are cross-sectional views illustrating various steps of a method according to a third exemplary embodiment of the present invention, ~~[sic]~~.

Description of the preferred embodiment.

Figures 1 through 8 show a method according to a first exemplary embodiment of the present invention. A thin silicon oxide layer was produced on a silicon substrate 1. This silicon oxide layer, that is not shown in Fig. 1, serves as a gate oxide during the further course of the method. Dependent on the application, silicon oxide layers of different thicknesses are employed in different regions of the silicon substrate. A polysilicon layer 2 is arranged on the silicon oxide layer. In this embodiment of the present invention, the polysilicon layer 2 was deposited as an undoped polysilicon layer, and is ~~this being~~ subsequently doped with the assistance of a photo technique. A silicon nitride layer 3 is arranged above the polysilicon layer 2. The thickness of the silicon nitride layer 3 ~~thereby~~ amounts to approximately 50 nm after the gate structuring. During the further course of the method, this layer serves as what is referred to as a "cap nitride".

Before producing the silicon oxide layer, a n-well 4 or, respectively, p-wells 5, 6 were produced in the silicon substrate. The individual wells are separated from one another by isolations 7. In the present example, these isolations 7 are fashioned as what are referred to as shallow trench isolations. The first region 8 of the silicon substrate 1 is arranged at the left side of Fig. 1. In this first region 8, the transistors from which the logic circuit is constructed are produced later. The second region 9 of the silicon substrate 1 is arranged at the right side of Fig. 1. In this second region 9, the transistors that serve as selection transistors in the memory cells are produced later. The structure produced by these steps is ~~shown~~ shown in Figure 1.

Subsequently, the silicon nitride layer 3 and the polysilicon layer 2 are structured on tracks by a photo technique to form gate paths 10, ~~(see Figure 2) with a photo technique~~. A re-oxidation of the gate in the first region 8 and gate paths 10' in the second region 9 (see Figure 2).

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oxide ~~ensues~~ in order to eliminate possible defects that occurred in the etching of the silicon nitride layer 3 and of the polysilicon layer 2. Phosphorous is now implanted into the silicon substrate with a photo technique for producing what are referred to as the source/drain regions 11 of the n-channel transistors. After this implantation, ~~a~~ ~~further~~ silicon nitride layer is deposited and is structured with an anisotropic etching. First insulating spacers, what are referred to as spacers 12, ~~arise at~~ the sidewalls of the gate paths 10 as a result of this etching. After producing the spacers 12, boron is implanted in the silicon substrate with a photo technique, so that the p-channel transistors can also be produced. Subsequently, a further silicon nitride layer 13 is deposited. The ~~situation deriving therefrom~~ is shown in Fig. 2.

The transistors that are produced in the second region 9 of the silicon substrate 1 serve as selection transistors in the memory cells. The capacitors of the memory cells, which are formed as trench capacitors in the present example, are not shown in the Figures for reasons of clarity. A high integration density arises particularly in the second region 9 of the silicon substrate 1. In order to be able to achieve this high integration density, a resist mask is produced that is opened at the locations at which the source/drain terminals, i.e. the terminals for the bit lines, the selection transistors, are produced ~~later~~. The silicon nitride layer 13 in the opening 14 of the mask 15 is removed with an anisotropic etching, ~~and~~ so that the source/drain regions 11 of the selection transistors are uncovered. The first region 8 of the silicon substrate 1 is ~~thereby~~ protected by the resist mask 15 and thus experiences no modification. Subsequently, the resist mask 15 is removed and a further polysilicon layer 16 is deposited. This polysilicon layer 16 is ~~a matter of~~ a doped polysilicon layer. ~~The situation deriving therefrom is shown in Figure 4.~~

The polysilicon layer 16 is now structured with the assistance of a further photo technique. The polysilicon layer 16 is ~~thereby~~ completely removed from the first region 8 of the silicon substrate 1. The remaining part of the polysilicon layer 16 forms what is referred to as a "landing pad" 17 in the second region 9 of the silicon substrate~~. The situation deriving therefrom is~~ shown in Fig. 5.

Subsequently, a further silicon oxide layer is deposited. This silicon oxide layer is structured ~~such with~~ a further anisotropic etching that a further spacer 18

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arises ~~at~~ on the spacer 12 on the sidewalls of the gate paths 10 in the first region 8 of the silicon substrate. As a result of the sequence of these spacers 12 and 18 ~~at~~ on the sidewalls of the gate paths 10 in the first region 8 of the silicon substrate and a suitably selected dopant implantations, the source/drain regions 11 of the transistors in the first region 8 can be set ~~such~~ so that transistors having extremely short switching times can be produced. Accordingly, extremely high-performance logic circuits can be constructed. Due to the polysilicon layer 16, no deposition of the silicon oxide layer between the gate paths 10' of the selection transistors occurs in the second region 9 of the silicon substrate. Accordingly, silicon oxide spacers 18 are also not produced between the gate paths 10' of the selection transistors. The area that is thereby saved between the gate paths 10' of the selection transistors can be used in order to arrange the gate paths correspondingly closer together, as a result whereof the integration density in the memory cell field is increased.

The remaining part of the silicon nitride layer 3 on the gate paths 10 in the first region 8 of the silicon substrate is removed with a further etching. This is possible because the silicon nitride layer 3 exhibits an extremely slight thickness in comparison to traditional methods. As a result of the removal of the silicon nitride layer 3, the gate paths 10 can now be doped in the desired type and fashion. A different doping of the various gate paths 10 is also possible in a simple way (dual work function gates). In this way, extremely fast logic circuits can be produced. The ~~situation deriving therefrom~~ structure formed by these steps is shown in Fig. 6.

Subsequently, a silicide-forming metal, for example tantalum, titanium, tungsten or cobalt, is sputtered on. A silicide reaction occurs on the uncovered silicon regions as a result of a thermal treatment, namely the gate paths in the first region as well as the uncovered source/drain regions, whereas the silicide-forming metal is preserved essentially unmodified in the other regions and can thereby be removed in turn in a simple way. The results are selective and self-aligned silicide layers 19 (See Figure 7) on the gate paths 10 in the first region 8 and the uncovered source/drain regions 11 ("salicide method"). The resistance of the gate paths 10 is clearly reduced by the silicide layers 19, ~~this having~~ and this has a positive influence on the performance capability of the logic circuit. ~~Further~~ In addition, the silicidation of the source/drain regions 11 clearly lowers the

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borophosilicate glasses

contact resistance, and this likewise ~~having~~ has a positive influence on the performance capability of the logic circuit.

Subsequently, a thin silicon nitride layer is deposited, and this ~~serving~~ layer serves as barrier. For reasons of clarity, this thin silicon nitride layer is not shown. This is followed by the deposition of ~~Borophosphosilicate~~ BPSG layer 20 that is planarized by a Chemical Mechanical Planarization or CMP step. A thermal treatment is implemented before the CMP step, so that the BPSG layer 20 can fill out the interspaces between the transistors as well as possible. The ~~situation~~ structures produced ~~deriving therefrom~~ by these steps is shown in Fig. 7.

Via holes 21 are now produced in the BPSG layer 20 with a further photo technique, as shown in Figure 8. These via holes 21 lead both to the silicon substrate 1 as well as to the gate paths 10. In the second region 9 of the silicon substrate, the via hole is conducted to the polysilicon layer 16 that serves as landing pad 17. After deposition of what is referred to as a liner (not shown), the via holes are filled with tungsten, and a CMP step is implemented in order to remove tungsten from the substrate surface outside the via holes.

For a complete production of the integrated circuit, the metalization as well as the passivation are subsequently constructed with a number of known steps. The inventive method has the advantage that the integration density in the second region of the semiconductor substrate can be clearly increased. Over and above this, the properties of the transistors in the first region of the semiconductor substrate can be clearly improved with little added outlay (silicidation, dual work function gates). The present invention, for example, therefore enables the cost-beneficial manufacture of what are referred to as embedded DRAM products.

Figs. 9 through 12 show a method according to a second exemplary embodiment of the present invention. The first steps of this method thereby agree with the steps shown in Figs. 1 through 4 and shall therefore not be repeated here.

In contrast to the first exemplary embodiment of the present invention, a relatively thick polysilicon layer is deposited. The polysilicon layer is structured with the assistance of a further photo technique. The polysilicon layer is thereby again completely removed from the first region of the silicon substrate. The remaining part

of the polysilicon layer forms the complete contact 24 in the second region of the silicon substrate. ~~The situation deriving therefrom is~~ shown in Fig. 9.

A further silicon oxide layer is subsequently deposited. This silicon oxide layer is structured ~~such with~~ a further anisotropic etching that a further spacer 18 ~~arises at~~ the sidewalls of the gate paths 10 in the first region 8 of the silicon substrate. Due to the contact 24, no deposition of the silicon oxide layer occurs in the second region 9 of the silicon substrate between the gate paths of the selection transistors. Accordingly, silicon oxide spacers 18 are also not produced between the gate paths 10 of the selection transistors. The area that is thereby ~~safe~~ between the gate paths 10 of the selection transistors can be utilized in order to arrange the gate paths 10 correspondingly closer together, as a result whereof the integration density in the memory cell field is increased.

The remaining ~~part~~ of the silicon nitride layer 3 on the gate paths ~~19~~ in the first region 8 as well as, partly in the second region 9 of the silicon substrate ~~is~~ removed with a further etching. This is possible because the silicon nitride layer 3 exhibits a very slight thickness compared to traditional methods. As a result of the removal of the silicon nitride layer 3, the gate paths 10 can now be doped in the desired way and fashion. A different doping of the various gate paths 10 is also possible in a simple way (dual work function gates). Very fast logic circuits can be produced in this way. The ~~situation deriving therefrom~~ is show in Fig. 10.

Subsequently, a silicide forming metal, for example tantalum, titanium, tungsten or cobalt is sputtered on. As a result of a thermal treatment, a silicide reaction occurs on the uncovered silicon regions, namely the gate paths 10 as well as the uncovered source/drain regions 11, whereas the silicide-forming metal remains essentially unmodified in the other regions and can therefore be simply removed in turn. The result are selective and self-aligned silicide layers 19 on the gate paths 10 and the uncovered source/drain regions 11 ("salicide method"). As a result of the silicide layers 19, the resistance of the gate paths 10 is clearly reduced, this ~~having~~ a positive effect on the performance capability of the logic circuit as well as of the word lines in the cell field. ~~Further~~, the contact resistance is clearly reduced due to the

silicidation of the source/drain regions 11, this likewise having a positive influence on the performance capability of the logic circuit.

Subsequently, a thin silicon nitride layer is deposited, this serving as barrier. For reasons of clarity, this thin silicon nitride layer is not shown. This is followed by the deposition of a BPSG layer 20 that is subjected to a thermal treatment so that the BPSG layer 20 can fill out the interspaces between the transistors as well as possible. Subsequently, the BPSG layer 20 is planarized with a CMP step. The CMP step is ~~thereby implanted such~~ implemented so that the contact 24 is uncovered. Only the first metallization layer therefore need be deposited in order to produce a conductive connection to the source/drain regions of the selection transistors in the memory cell field. This ~~situation deriving therefrom~~ structure is shown in Fig. 11.

Via holes 21 are now produced in the BPSG layer 20 with a further photo technique. These via holes 21 lead both to the silicon substrate of the remaining transistors as well as to the gate paths 10. After deposition of what is referred to as a liner (not shown), the via holes are filled with tungsten and a CMP step is implemented in order to remove tungsten from the substrate surface outside the via holes 21. The ~~situation deriving therefrom~~ structure which is produced by these steps is shown in Fig. 12.

For complete manufacture of the integrated circuit, the metallization as well as the passivation are built up again with a number of known steps. This inventive method also has the advantage that the integration density in the second region of the semiconductor substrate can be clearly increased. Over and above this, the properties of the transistors in the first region of the semiconductor substrate can be clearly improved with a slight added outlay (silicidation, dual work function gates).

Figures 13 through 18 show a method according to a third exemplary embodiment of the present invention. In contrast to the first exemplary embodiment of the present invention, however, the polysilicon layer does not serve as a landing pad but what is referred to as a sacrificial contact.

A thin silicon oxide layer is produced on a silicon substrate 1. This silicon oxide layer, which is not shown in Figure 13, serves as gate oxide during the further course of the method. A polysilicon layer 2 is arranged on the silicon oxide layer. In this embodiment of the present invention, the polysilicon layer 2 was deposited as an

undoped polysilicon layer, ~~this being~~ and is subsequently doped with the assistance of a photo technique. A silicon nitride layer 3 is arranged over the polysilicon layer 2. The thickness of the silicon nitride layer 3 ~~thereby~~ amounts to approximately 50 nm.

Before producing the silicon oxide layer, an n-well 4 or, respectively, p-wells 5, 6 are produced in the silicon substrate. The individual wells are thereby separated from one another by isolations 7. These isolations 7 are formed as what are referred to as shallow trench isolations in the present example. The silicon substrate is again divided into a first region 8 and into a second region 9 as shown in Figure 13.

Subsequently, the silicon nitride layer 3 and the polysilicon layer 2 are structured with a photo technique in the first region 8 and gate paths 10' in the second region 9 to form gate paths 10 ~~with a photo technique~~. A re-oxidation of the gate oxide follows in order to eliminate possible defects that occurred in the etching of the silicon nitride layer 3 and of the polysilicon layer 2. Phosphorous is now implanted in the silicon substrate with a photo technique in order to produce what are referred to as source/drain regions 11 of the n-channel transistors. A further silicon nitride layer is deposited after this implantation and is structured with an anisotropic etching. First insulating spacers 12 are formed on ~~arise at~~ the sidewalls of the gate paths 10 as a result of this etching. After producing the spacers 12, boron is implanted into the silicon substrate with a photo technique, so that the p-channel transistors can also be produced. Subsequently, a further silicon nitride layer 13 is deposited. The ~~situation deriving~~ structure which is formed by these steps ~~therefrom~~ is shown in Figure 14.

A further polysilicon layer 16 is subsequently deposited as shown in Figure 15. This polysilicon layer 16 is ~~a matter of~~ an undoped polysilicon layer that later forms the sacrificial contact. ~~The situation deriving therefrom is shown in Fig. 15.~~

The polysilicon layer 16 is ~~not~~ now structured with the assistance of a further photo technique. The polysilicon layer 16 is thereby completely removed from the first region 8 of the silicon substrate 1. The remaining part of the polysilicon layer 16 forms the sacrificial contact 25 in the second region 9 of the silicon substrate. ~~The situation deriving therefrom is~~ As shown in Figure 16.

A further silicon oxide layer is subsequently deposited. This silicon oxide layer is structured ~~such~~ so with a further anisotropic etching that ~~a~~ further spacers 18, which are made up of parts of the layer 13 and the silicon oxide layer are formed on the spacers 12 on ~~arises at~~ the sidewalls of the gate paths 10 in the first region 8 of the silicon substrate.

Due to the sequence of these spacers 12 and 18 ~~at~~ on the sidewalls of the gate paths 10 in the first region 8 of the silicon substrate and a suitably selected dopant implantations, the source/drain regions 11 of the transistors in the first region 8 can be set ~~such~~ so that transistors having extremely short switching times can be produced. Accordingly, extremely high-performance logic circuits can be constructed. Due to the sacrificial contact 25, no deposition of the silicon oxide layer occurs between the gate paths 10' of the selection transistors in the second region 9 of the silicon substrate. Accordingly, silicon oxide spacers 18 are also not produced between the gate paths 10 of the selection transistors. The area between the gate paths 10' of the selection transistors that is ~~thereby~~ saved can be used in order to arrange the gate paths correspondingly closer together, so that the integration density in the memory cell field is increased as a result thereof.

The remaining part of the silicon nitride layer 3 on the gate paths 10 in the first region 8 of the silicon substrate is also removed with a further etching. This is possible because the silicon nitride layer 3 exhibits an extremely slight thickness compared to traditional methods. The gate paths 10 can now be doped in the desired way and fashion as a result of the removal of the silicon nitride layer 3. Subsequently, a ~~silicon-forming~~ silicide forming metal, for example tantalum, titanium, tungsten or cobalt, is sputtered on. As a result of a thermal treatment, a silicide reaction occurs on the uncovered silicon regions, namely the gate paths 10 in the first region 8 as well as the uncovered source/drain regions 11, whereas the silicide-forming metal remains essentially unmodified in the other regions and can thereby be removed in turn in a simple way. The result are selective and self-aligned silicide layers 19 on the gate paths 10 in the first region and the uncovered source/drain regions 11 ("salicide method").

The deposition of a BPSG layer 20 follows, ~~this being~~ and is planarized with a CMP step. A thermal treatment is implemented before the CMP step so that the BPSG layer 20 can fill up the interspaces between the transistors as well as possible. The ~~situation deriving therefrom~~ structure which is formed by these steps is shown in Fig. 17.

Via holes 21 are now produced in the BPSG layer 20 with a further photo technique. These via holes 21 lead both to the silicon substrate as well as to the gate

paths 10 in the third region 8. The via hole is conducted to the sacrificial contact 25 in the second region 9 of the silicon substrate. A part of the sacrificial contact 25 and the silicon nitride layer 13 that still remains is removed with a dry-chemical or wet-chemical etching, so that there is now a space for the actual contact. This etching of the sacrificial contact 25 can be implemented with high selectivity relative to the surrounding material.

A deposition of what is referred to as a liner (not shown) and the deposition of a tungsten layer that serves the purpose of filling up the via holes again ~~ensue~~ occur. In a further CMP step, the tungsten that is located outside the via holes is removed from the substrate surface. The ~~situation deriving therefrom~~ structure which is formed by these steps is shown in Figure 18.

Due to the employment of the sacrificial contact 25, ~~a mask level~~ masking and etching step can be eliminated compared to the first embodiment because the silicon nitride 13 need not be removed ~~with a mask~~ between selection transistors in the second region 9.

MARKED-UP VERSION

List of Reference Characters

1	silicon substrate
2	polysilicon
3	silicon nitride layer
4	n-well
5	p-well
6	p-well
7	insulation
8	first region
9	second region
10	gate path
11	source/drain regions
12	spacer
13	silicon nitride layer
14	opening
15	resist mask
16	polysilicon
17	landing pad
18	spacer
19	silicide layer
20	BPSG layer
21	via holes
22	...
23	...
24	contact
25	sacrificial contact

We claim

~~Patent Claims~~

1. Method for producing an integrated semiconductor component comprising the steps:

a) a semiconductor substrate having at least one first region and at least one second region is prepared;

b) gate paths are produced in the first and in the second region of the semiconductor substrate;

c) source/drain regions neighboring the gate paths and at least two spacers at the gate paths are produced in the first region of the semiconductor substrate;

d) source/drain regions are produced neighboring the gate paths in the second region of the semiconductor substrate, and, for preparing the contacts to predetermined source/drain regions in the second region of the semiconductor substrate, sacrificial contacts are formed before all spacers have been produced in the first region of the semiconductor substrate.

2. Method according to claim 1, characterized in that the spacers are formed of silicon oxide, silicon nitride or oxynitride.

3. Method according to claim 1 or 2, characterized in that the gate paths are formed in that a polysilicon layer and a protective layer, particularly a silicon nitride, silicon oxide or oxynitride layer, are generated and these layers are structured in common to form gate paths.

4. Method according to claim 3, characterized in that the protective layer is generated with a thickness such that the protective layer exhibits a thickness of less than 100 nm after the gate structuring.

5. Method according to one of the preceding claims, the gate paths in the first region of the semiconductor substrate are doped with dopants having different conductivity types.

6. Method according to one of the preceding claims, characterized in that silicide layers are generated on the gate paths in the first region of the semiconductor substrate.

9/prts

METHOD FOR PRODUCING INTEGRATED SEMICONDUCTOR COMPONENTS

The present invention is directed to a method for producing an integrated semiconductor component. In particular, the present invention is directed to a method for producing and integrated DRAM or embedded DRAM or, respectively, embedded SRAM semiconductor component.

The goal of many developments in microelectronics is to constantly lower the costs to be expended for the realization of a specific electronic function and, thus, to constantly increase the productivity. The guarantee for increasing productivity in recent years was and is, thereby, the constant structural miniaturization of the semiconductor components. In particular, field effect transistors are being constantly miniaturized and arranged in integrated circuits having the highest packing density.

In order to carry out their function, field effect transistors must be connected to other field effect transistors and to the outside world. To that end, contacts to the diffusion regions of the transistors must be produced. In methods for manufacturing logic circuits, for example, via holes to the diffusion regions of the transistors are produced by a photo technique and an etching. Since this formation of the via holes is usually not implemented self-aligned, an adequately large safety margin between the gate track and the via hole must be adhered to; this, of course, has a negative influence on the integration density.

In methods for producing DRAM semiconductor components, self-aligned contacts are usually produced. Via holes are thereby usually etched in a BPSG layer deposited between the gate paths. Subsequently, these via holes are filled with a conductive material, so that a conductive connection is created.

The production of these via holes, however, becomes more and more difficult with ongoing structural miniaturization. In modern field effect transistors, a number of spacers are produced at the sidewalls of the gate webs, these, in interaction with suitable dopant implantations, seeing to it that it dopant profiles suitable for the respective purpose can be produced in the source/drain regions. Due to the spacers arranged between the gate paths and the demand that the via hole should be arranged

between the spacers insofar as possible, the distance between the gate paths or, respectively, the diffusion region that serves the purpose of contacting must be selected adequately large, this having a negative influence on the integration density that can be achieved.

When etching the via holes, the gate paths dare not be damaged, since a short would otherwise arise between the diffusion contact and the gate. Since, despite all efforts, one cannot prevent the gate paths from being attacked when etching the via holes, a thick protective layer, was referred to as a "cap", is usually arranged on the gate paths, this being intended to prevent a short between contact and gate. The relatively great thickness of this protective layer, however, deteriorates the quality of the gate paths and usually prevents a silicidization of the gate paths as well as the subsequent doping of the polysilicon of the gate paths (dual work function gate).

Due to the tight conditions between the gate paths, it is necessary that the insulation layer be subjected to a temperature treatment at relatively high temperatures in order to achieve a flowing of the insulation layer. Nonetheless, holes, what are referred to as voids, can occur between the gate paths in the deposition of the insulation layer. When the via holes are then formed, it can occur that two via holes are connected to one another via a void. In the subsequent filling of the via holes with conductive material, the voids are usually also filled, so that a short between two contacts can arise that possibly leads to the outage of the entire circuit.

It is therefore the object of the present invention to offer a method for producing an integrated semiconductor component that minimizes or, respectively, entirely avoids said problems.

This object is inventively achieved by the methods for producing an integrated semiconductor component according to independent patent claims 1 or 3. Further advantageous embodiments, properties and aspects of the present invention derive from the dependent claims, from the specification and from the attached drawings.

Inventively, a method for producing an integrated semiconductor component is offered that comprises the following steps:

a) a semiconductor substrate having at least one first region and at least one second region is prepared;

b) gate paths are produced in the first and in the second region of the semiconductor substrate;

c) source/drain regions neighboring the gate paths and at least two spacers at the gate paths are produced in the first region of the semiconductor substrate;

d) source/drain regions are produced neighboring the gate paths in the second region of the semiconductor substrate, and contacts to predetermined source/drain regions are formed before all spacers have been produced in the first region of the semiconductor substrate.

Inventively, a method for producing an integrated semiconductor component having the following steps is also offered:

a) a semiconductor substrate having at least one first region and at least one second region is prepared;

b) gate paths are produced in the first and in the second region of the semiconductor substrate;

c) source/drain regions neighboring the gate paths as well as at least two spaces at the gate paths are produced in the first region of the semiconductor substrate;

d) source/drain regions neighboring the gate paths are produced in the second region of the semiconductor substrate, and contacts to predetermined source/drain regions are prepared before all spacers in the first region of the semiconductor substrate have been produced.

The inventive methods have the advantage that integration density in the second region of the semiconductor substrate can be noticeably increased. As a result of the feature that the formation of the contacts to the source/drain regions is undertaken or, respectively, readied in the second region of the semiconductor substrate at a time at which all spacers have not yet been produced, no unnecessary

spacer production occurs in the second region, as a result whereof chip area can be saved. The saved area can, for example, be used in order to arrange the gate paths closer together in the second region. The spacers can thereby be employed as an aid for setting the desired dopant profiles and/or as lateral insulation of the gate paths.

Further, the inventive methods can be integrated without difficulty in a process sequence that already exists for producing a semiconductor component. In particular, the process steps for the manufacture of very fast logic circuits can be retained nearly unmodified. Problems such as derive at traditional methods due to the occurrence of voids between the transistors can be clearly reduced or, respectively, entirely avoided given the inventive methods. Due to the early formation or, respectively, preparation of the contacts, high aspect ratios can be avoided, as a result whereof, the processes can be implemented more stably overall. The contacts can thereby also already be formed or, respectively, prepared at a time at which the source/drain regions have not yet been formed at all.

According to a preferred embodiment, landing pads are formed in the second region of the semiconductor substrate for preparing the contacts to predetermined source/drain regions. Doped polysilicon is preferably employed for forming the landing pads or, respectively, the contacts themselves.

According to another preferred embodiment, sacrificial contacts are formed in the second region of the semiconductor substrate for preparing the contacts to predetermined source/drain regions. The sacrificial contacts likewise prevent the production of unnecessary spacers at the gate paths in the second region of the semiconductor substrate. They are removed only when the actual contacts to the source/drain regions are formed.

According to a preferred embodiment, the spacers are formed of silicon oxide, silicon nitride or oxynitride. To that end, a silicon oxide layer, silicon nitride layer or oxynitride layer is deposited over the gate paths and etched back with an anisotropic etching, so that parts of these layers remain at the sidewalls of the gate paths. By employing these spacers, the dopings of the source/drain region can be set very precisely corresponding to the respective demands.

According to another preferred embodiment, the gate paths are formed in that a polysilicon layer and a protective layer, particularly a silicon nitride layer, silicon oxide layer or oxynitride layer is produced and these layers are structured in common to form gate paths. It is thereby particularly preferred when the protective layer is produced with a thickness such that the protective layer comprises a thickness less than 100 nm, preferably between 40 and 60 nm, after the gate structuring. This protective layer is frequently referred to as "cap" and, in traditional processes, serves among other things as a hard mask for gate structuring and for protecting the gate paths in an etching process for producing the via holes. In the prior art, a dry-etching process that etches oxide selectively relative to the cap material must be utilized for this purpose. Since the structure to be etched exhibits a high aspect ratio in the prior art, the selectivity of the etching process is not very high, and a relatively thick "cap" must be employed in order to avoid a short between the gate path and the contact.

Since the formation of the contact is already undertaken or, respectively, prepared at a very early stage given the inventive methods, the "cap" now serves only for insulating the gate path from the contact and can therefore be selected relatively thin. Accordingly, the "cap" can be completely removed from the gate paths in the first region in later process steps, for example when etching a nitride spacer, and without additional process steps, this opening up the possibility of doping various gate paths with different dopants and thus constructing what are referred to as dual work function gates. Further, the gate paths can be silicided in this way, as a result whereof the resistance of the gate paths is clearly reduced.

It is also preferred when the gate paths in the first region of the semiconductor substrate are doped with dopants having different conductivity types. As a result of what is referred to as these dual work function gates, extremely high-performance logic circuits can be constructed. In this way, the supply voltage can also be reduced without incurring any losses in the switching speed.

For reducing the resistances of the gate paths, it is preferred when silicide layers are produced on the gate paths in the first region of the semiconductor substrate. In particular, it is preferred when $CoSi_2$, $TaSi_2$, $TiSi_2$ or WSi_x is employed as silicide layers, and these silicide layers are produced by a salicide method.

The invention is explained in greater detail below with reference to the drawings. Shown are:

Figs. 1 - 8 a method according to a first exemplary embodiment of the present invention;

Figs. 9 - 12 a method according to a second exemplary embodiment of the present invention;

Figs. 13-18 a method according to a third exemplary embodiment of the present invention, [sic]

Figures 1 through 8 show a method according to a first exemplary embodiment of the present invention. A thin silicon oxide layer was produced on a silicon substrate 1. This silicon oxide layer, that is not shown in Fig. 1, serves as gate oxide during the further course of the method. Dependent on the application, silicon oxide layers of different thicknesses are employed in different regions of the silicon substrate. A polysilicon layer 2 is arranged on the silicon oxide layer. In this embodiment of the present invention, the polysilicon layer 2 was deposited as an undoped polysilicon layer, this being subsequently doped with the assistance of a photo technique. A silicon nitride layer 3 is arranged above the polysilicon layer 2. The thickness of the silicon nitride layer 3 thereby amounts to approximately 50 nm after the gate structuring. During the further course of the method, this layer serves as what is referred to as a "cap nitride".

Before producing the silicon oxide layer, a n-well 4 or, respectively, p-wells 5, 6 were produced in the silicon substrate. The individual wells are separated from one another by isolations 7. In the present example, these isolations 7 are fashioned as what are referred to as shallow trench isolations. The first region 8 of the silicon substrate 1 is arranged at the left side of Fig. 1. In this first region 8, the transistors from which the logic circuit is constructed are produced later. The second region 9 of the silicon substrate 1 is arranged at the right side of Fig. 1. In this second region 9, the transistors that serve as selection transistors in the memory cells are produced later.

Subsequently, the silicon nitride layer 3 and the polysilicon layer 2 are structured to form gate paths 10 with a photo technique. A re-oxidation of the gate

oxide ensues in order to eliminate possible defects that occurred in the etching of the silicon nitride layer 3 and of the polysilicon layer 2. Phosphorous is now implanted into the silicon substrate with a photo technique for producing what are referred to as the source/drain regions 11 of the n-channel transistors. After this implantation, a further silicon nitride layer is deposited and is structured with an anisotropic etching. First insulating spacers, what are referred to as spacers 12, arise at the sidewalls of the gate paths 10 as a result of this etching. After producing the spacers 12, boron is implanted in the silicon substrate with a photo technique, so that the p-channel transistors can also be produced. Subsequently, a further silicon nitride layer 13 is deposited. The situation deriving therefrom is shown in Fig. 2.

The transistors that are produced in the second region 9 of the silicon substrate 1 serve as selection transistors in the memory cells. The capacitors of the memory cells, which are formed as trench capacitors in the present example, are not shown in the Figures for reasons of clarity. A high integration density arises particularly in the second region 9 of the silicon substrate 1. In order to be able to achieve this high integration density, a resist mask is produced that is opened at the locations at which the source/drain terminals, i.e. the terminals for the bit lines, the selection transistors, are produced later. The silicon nitride layer 13 in the opening 14 of the mask 15 is removed with an anisotropic etching, and so that the source/drain regions 11 of the selection transistors are uncovered. The first region 8 of the silicon substrate 1 is thereby protected by the resist mask 15 and thus experiences no modification. Subsequently, the resist mask 15 is removed and a further polysilicon layer 16 is deposited. This polysilicon layer 16 is a matter of a doped polysilicon layer. The situation deriving therefrom is shown in Figure 4.

The polysilicon layer 16 is now structured with the assistance of a further photo technique. The polysilicon layer 16 is thereby completely removed from the first region 8 of the silicon substrate 1. The remaining part of the polysilicon layer 16 forms what is referred to as a "landing pad" 17 in the second region 9 of the silicon substrate. The situation deriving therefrom is shown in Fig. 5.

Subsequently, a further silicon oxide layer is deposited. This silicon oxide layer is structured such with a further anisotropic etching that a further spacer 18

arises at the sidewalls of the gate paths 10 in the first region 8 of the silicon substrate. As a result of the sequence of these spacers 12 and 18 at the sidewalls of the gate paths 10 in the first region 8 of the silicon substrate and suitably selected dopant implantations, the source/drain regions 11 of the transistors in the first region 8 can be set such that transistors having extremely short switching times can be produced. Accordingly, extremely high-performance logic circuits can be constructed. Due to the polysilicon layer 16, no deposition of the silicon oxide layer between the gate paths of the selection transistors occurs in the second region 9 of the silicon substrate. Accordingly, silicon oxide spacers 18 are also not produced between the gate paths 10 of the selection transistors. The area that is thereby saved between the gate paths of the selection transistors can be used in order to arrange the gate paths correspondingly closer together, as a result whereof the integration density in the memory cell field is increased.

The remaining part of the silicon nitride layer 3 on the gate paths 10 in the first region 8 of the silicon substrate is removed with a further etching. This is possible because the silicon nitride layer 3 exhibits an extremely slight thickness in comparison to traditional methods. As a result of the removal of the silicon nitride layer 3, the gate paths 10 can now be doped in the desired type and fashion. A different doping of the various gate paths 10 is also possible in a simple way (dual work function gates). In this way, extremely fast logic circuits can be produced. The situation deriving therefrom is shown in Fig. 6.

Subsequently, a silicide-forming metal, for example tantalum, titanium, tungsten or cobalt, is sputtered on. A silicide reaction occurs on the uncovered silicon regions as a result of a thermal treatment, namely the gate paths in the first region as well as the uncovered source/drain regions, whereas the silicide-forming metal is preserved essentially unmodified in the other regions and can thereby be removed in turn in a simple way. The results are selective and self-aligned silicide layers 19 on the gate paths in the first region 8 and the uncovered source/drain regions 11 ("salicide method"). The resistance of the gate paths 10 is clearly reduced by the silicide layers 19, this having a positive influence on the performance capability of the logic circuit. Further, the silicidation of the source/drain regions 11 clearly lowers the

contact resistance, this likewise having a positive influence on the performance capability of the logic circuit.

Subsequently, a thin silicon nitride layer is deposited, this serving as barrier. For reasons of clarity, this thin silicon nitride layer is not shown. This is followed by the deposition of BPSG layer 20 that is planarized by a CMP step. A thermal treatment is implemented before the CMP step, so that the BPSG layer 20 can fill out the interspaces between the transistors as well as possible. The situation deriving therefrom is shown in Fig. 7.

Via holes 21 are now produced in the BPSG layer 20 with a further technique. These via holes 21 lead both to the silicon substrate 1 as well as to the gate paths 10. In the second region 9 of the silicon substrate, the via hole is conducted to the polysilicon layer 16 that serves as landing pad 17. After deposition of what is referred to as a liner (not shown), the via holes are filled with tungsten, and a CMP step is implemented in order to remove tungsten from the substrate surface outside the via holes.

For a complete production of the integrated circuit, the metalization as well as the passivation are subsequently constructed with a number of known steps. The inventive method has the advantage that the integration density in the second region of the semiconductor substrate can be clearly increased. Over and above this, the properties of the transistors in the first region of the semiconductor substrate can be clearly improved with little added outlay (silicidation, dual work function gates). The present invention, for example, therefore enables the cost-beneficial manufacture of what are referred to as embedded DRAM products.

Figs. 9 through 12 show a method according to a second exemplary embodiment of the present invention. The first steps of this method thereby agree with the steps shown in Figs. 1 through 4 and shall therefore not be repeated here.

In contrast to the first exemplary embodiment of the present invention, a relatively thick polysilicon layer is deposited. The polysilicon layer is structured with the assistance of a further photo technique. The polysilicon layer is thereby again completely removed from the first region of the silicon substrate. The remaining part

of the polysilicon layer forms the complete contact 24 in the second region of the silicon substrate. The situation deriving therefrom is shown in Fig. 9.

A further silicon oxide layer is subsequently deposited. This silicon oxide layer is structured such with a further anisotropic etching that a further spacer 18 arises at the sidewalls of the gate paths 10 in the first region 8 of the silicon substrate. Due to the contact 24, no deposition of the silicon oxide layer occurs in the second region 9 of the silicon substrate between the gate paths of the selection transistors. Accordingly, silicon oxide spacers 18 are also not produced between the gate paths 10 of the selection transistors. The area that is thereby safe between the gate paths 10 of the selection transistors can be utilized in order to arrange the gate paths 10 correspondingly closer together, as a result whereof the integration density in the memory cell field is increased.

The remaining part of the silicon nitride layer 3 on the gate paths 19 in the first region 8 as well as, partly, in the second region 9 of the silicon substrate is removed with a further etching. This is possible because the silicon nitride layer 3 exhibits a very slight thickness compared to traditional methods. As a result of the removal of the silicon nitride layer 3, the gate paths 10 can now be doped in the desired way and fashion. A different doping of the various gate paths 10 is also possible in a simple way (dual work function gates). Very fast logic circuits can be produced in this way. The situation deriving therefrom is show in Fig. 10.

Subsequently, a silicide forming metal, for example tantalum, titanium, tungsten or cobalt is sputtered on. As a result of a thermal treatment, a silicide reaction occurs on the uncovered silicon regions, namely the gate paths 10 as well as the uncovered source/drain regions 11, whereas the silicide-forming metal remains essentially unmodified in the other regions and can therefore be simply removed in turn. The result are selective and self-aligned silicide layers 19 on the gate paths 10 and the uncovered source/drain regions 11 ("salicide method"). As a result of the silicide layers 19, the resistance of the gate paths 10 is clearly reduced, this having a positive effect on the performance capability of the logic circuit as well as of the word lines in the cell field. Further, the contact resistance is clearly reduced due to the

silicidation of the source/drain regions 11, this likewise having a positive influence on the performance capability of the logic circuit.

Subsequently, a thin silicon nitride layer is deposited, this serving as barrier. For reasons of clarity, this thin silicon nitride layer is not shown. This is followed by the deposition of a BPSG layer 20 that is subjected to a thermal treatment so that the BPSG layer 20 can fill out the interspaces between the transistors as well as possible. Subsequently, the BPSG layer 20 is planarized with a CMP step. The CMP step is thereby implanted such that the contact 24 is uncovered. Only the first metallization layer therefore need be deposited in order to produce a conductive connection to the source/drain regions of the selection transistors in the memory cell field. This situation deriving therefrom is shown in Fig. 11.

Via holes 21 are now produced in the BPSG layer 20 with a further photo technique. These via holes 21 lead both to the silicon substrate of the remaining transistors as well as to the gate paths 10. After deposition of what is referred to as a liner (not shown), the via holes are filled with tungsten and a CMP step is implemented in order to remove tungsten from the substrate surface outside the via holes 21. The situation deriving therefrom is shown in Fig. 12.

For complete manufacture of the integrated circuit, the metallization as well as the passivation are built up again with a number of known steps. This inventive method also has the advantage that the integration density in the second region of the semiconductor substrate can be clearly increased. Over and above this, the properties of the transistors in the first region of the semiconductor substrate can be clearly improved with a slight added outlay (silicidation, dual work function gates).

Figures 13 through 18 show a method according to a third exemplary embodiment of the present invention. In contrast to the first exemplary embodiment of the present invention, however, the polysilicon layer does not serve as landing pad but what is referred to as a sacrificial contact.

A thin silicon oxide layer is produced on a silicon substrate 1. This silicon oxide layer, which is not shown in Figure 13, serves as gate oxide during the further course of the method. A polysilicon layer 2 is arranged on the silicon oxide layer. In this embodiment of the present invention, the polysilicon layer 2 was deposited as an

undoped polysilicon layer, this being subsequently doped with the assistance of a photo technique. A silicon nitride layer 3 is arranged over the polysilicon layer 2. The thickness of the silicon nitride layer 3 thereby amounts to approximately 50 nm.

Before producing the silicon oxide layer, an n-well 4 or, respectively, p-wells 5, 6 are produced in the silicon substrate. The individual wells are thereby separated from one another by isolations 7. These isolations 7 are formed as what are referred to as shallow trench isolations in the present example. The silicon substrate is again divided into a first and into a second region.

Subsequently, the silicon nitride layer 3 and the polysilicon layer 2 are structured to form gate paths 10 with a photo technique. A re-oxidation of the gate oxide follows in order to eliminate possible defects that occurred in the etching of the silicon nitride layer 3 and of the polysilicon layer 2. Phosphorous is now implanted in the silicon substrate with a photo technique in order to produce what are referred to as source/drain regions 11 of the n-channel transistors. A further silicon nitride layer is deposited after this implantation and is structured with an anisotropic etching. First insulating spacers 12 arise at the sidewalls of the gate paths 10 as a result of this etching. After producing the spacers 12, boron is implanted into the silicon substrate with a photo technique, so that the p-channel transistors can also be produced. Subsequently, a further silicon nitride layer 13 is deposited. The situation deriving therefrom is shown in Figure 14.

A further polysilicon layer 16 is subsequently deposited. This polysilicon layer 16 is a matter of an undoped polysilicon layer that later forms the sacrificial contact. The situation deriving therefrom is shown in Fig. 15.

The polysilicon layer 16 is not structured with the assistance of a further photo technique. The polysilicon layer 16 is thereby completely removed from the first region 8 of the silicon substrate 1. The remaining part of the polysilicon layer 16 forms the sacrificial contact 25 in the second region 9 of the silicon substrate. The situation deriving therefrom is shown in Figure 16.

A further silicon oxide layer is subsequently deposited. This silicon oxide layer is structured such with a further anisotropic etching that a further spacer 18 arises at the sidewalls of the gate paths 10 in the first region 8 of the silicon substrate.

Due to the sequence of these spacers 12 and 18 at the sidewalls of the gate paths 10 in the first region of the silicon substrate and suitably selected dopant implantations, the source/drain regions 11 of the transistors in the first region 8 can be set such that transistors having extremely short switching times can be produced. Accordingly, extremely high-performance logic circuits can be constructed. Due to the sacrificial contact 25, no deposition of the silicon oxide layer occurs between the gate paths of the selection transistors in the second region 9 of the silicon substrate. Accordingly, silicon oxide spacers 18 are also not produced between the gate paths 10 of the selection transistors. The area between the gate paths of the selection transistors that is thereby saved can be used in order to arrange the gate paths correspondingly closer together, the integration density in the memory cell field being increased as a result thereof.

The remaining part of the silicon nitride layer 3 on the gate paths 10 in the first region 8 of the silicon substrate is also removed with a further etching. This is possible because the silicon nitride layer 3 exhibits an extremely slight thickness compared to traditional methods. The gate paths 10 can now be doped in the desired way and fashion as a result of the removal of the silicon nitride layer 3. Subsequently, a silicon-forming metal, for example tantalum, titanium, tungsten or cobalt, is sputtered on. As a result of a thermal treatment, a silicide reaction occurs on the uncovered silicon regions, namely the gate paths 10 in the first region 8 as well as the uncovered source/drain regions 11, whereas the silicide-forming metal remains essentially unmodified in the other regions and can thereby be removed in turn in a simple way. The result are selective and self-aligned silicide layers 19 on the gate paths 10 in the first region and the uncovered source/drain regions 11 ("salicide method").

The deposition of a BPSG layer 20 follows, this being planarized with a CMP step. A thermal treatment is implemented before the CMP step so that the BPSG layer 20 can fill up the interspaces between the transistors as well as possible. The situation deriving therefrom is shown in Fig. 17.

Via holes 21 are now produced in the BPSG layer 20 with a further photo technique. These via holes 21 lead both to the silicon substrate as well as to the gate

paths 10. The via hole is conducted to the sacrificial contact 25 in the second region 9 of the silicon substrate. A part of the sacrificial contact 25 and the silicon nitride layer 13 that still remains is removed with a dry-chemical or wet-chemical etching, so that there is now a space for the actual contact. This etching of the sacrificial contact 25 can be implemented with high selectivity relative to the surrounding material.

A deposition of what is referred to as a liner (not shown) and the deposition of a tungsten layer that serves the purpose of filling up the via holes again ensue. In a further CMP step, the tungsten that is located outside the via holes is removed from the substrate surface. The situation deriving therefrom is shown in Figure 18.

Due to the employment of the sacrificial contact 25, a mask level can be eliminated compared to the first embodiment because the silicon nitride 13 need not be removed with a mask between selection transistors in the second region 9.

List of Reference Characters

1	silicon substrate
2	polysilicon
3	silicon nitride layer
4	n-well
5	p-well
6	p-well
7	insulation
8	first region
9	second region
10	gate path
11	source/drain regions
12	spacer
13	silicon nitride layer
14	opening
15	resist mask
16	polysilicon
17	landing pad
18	spacer
19	silicide layer
20	BPSG layer
21	via holes
22	...
23	...
24	contact
25	sacrificial contact

Patent Claims

1. Method for producing an integrated semiconductor component comprising the steps:

a) a semiconductor substrate having at least one first region and at least one second region is prepared;

b) gate paths are produced in the first and in the second region of the semiconductor substrate;

c) source/drain regions neighboring the gate paths and at least two spacers at the gate paths are produced in the first region of the semiconductor substrate;

d) source/drain regions are produced neighboring the gate paths in the second region of the semiconductor substrate, and contacts to predetermined source/drain regions are formed before all spacers have been produced in the first region of the semiconductor substrate.

2. Method according to claim 1, characterized in that polysilicon is employed for forming the contacts to predetermined source/drain regions in the second region of the semiconductor substrate.

3. Method for producing an integrated semiconductor component comprising the steps:

a) a semiconductor substrate having at least one first region and at least one second region is prepared;

b) gate paths are produced in the first and in the second region of the semiconductor substrate;

c) source/drain regions neighboring the gate paths as well as at least two spaces at the gate paths are produced in the first region of the semiconductor substrate;

d) source/drain regions neighboring the gate paths are produced in the second region of the semiconductor substrate, and contacts to predetermined source/drain regions are prepared before all spacers

in the first region of the semiconductor substrate have been produced.

4. Method according to claim 3, characterized in that landing pads are formed for preparing the contacts to predetermined source/drain regions in the second region of the semiconductor substrate.

5. Method according to claim 4, characterized in that polysilicon is employed for forming the landing pads.

6. Method according to claim 3, characterized in that sacrificial contacts are formed for preparing the contacts to predetermined source/drain regions in the second region of the semiconductor substrate.

7. Method according to one of the preceding claims, characterized in that the spacers are formed of silicon oxide, silicon nitride or oxynitride.

8. Method according to one of the preceding claims, characterized in that the gate paths are formed in that a polysilicon layer and a protective layer, particularly a silicon nitride, silicon oxide or oxynitride layer, are generated and these layers are structured in common to form gate paths.

9. Method according to claim 8, characterized in that the protective layer is generated with a thickness such that the protective layer exhibits a thickness of less than 100 nm after the gate structuring.

10. Method according to one of the preceding claims, the gate paths in the first region of the semiconductor substrate are doped with dopants having different conductivity types.

11. Method according to one of the preceding claims, characterized in that silicide layers are generated on the gate paths in the first region of the semiconductor substrate.

12. Method according to claim 11, characterized in that $CoSi_2$, $TaSi_2$, $TiSi_2$ or WSi_x are employed as silicide layers.

13. Method according to claim 11 or 12, characterized in that the silicide layers are produced with a salicide method.

14. Semiconductor component, characterized in that the semiconductor component can be manufactured with a method according to one of the preceding claims.

TITLE

"METHOD FOR PRODUCING INTEGRATED SEMICONDUCTOR COMPONENTS"

BACKGROUND OF THE INVENTION

The present invention is directed to a method for producing an integrated semiconductor component. In particular, the present invention is directed to a method for producing either an integrated DRAM, an embedded DRAM or, respectively, an embedded SRAM semiconductor component.

The goal of many developments in microelectronics is to constantly lower the costs to be expended for the realization of a specific electronic function and, thus, to constantly increase the productivity. The guarantee for increasing productivity in recent years was and is, thereby, the constant structural miniaturization of the semiconductor components. In particular, field effect transistors are being constantly miniaturized and arranged in integrated circuits having the highest packing density.

In order to carry out their function, field effect transistors must be connected to other field effect transistors and to the outside world. To that end, contacts to the diffusion regions of the transistors must be produced. In methods for manufacturing logic circuits, for example, via holes to the diffusion regions of the transistors are produced by a photo technique and an etching. Since this formation of the via holes is usually not implemented to be self-aligned, an adequately large safety margin between the gate track and the via hole must be provided and this margin, of course, has a negative influence on the integration density.

In methods for producing DRAM semiconductor components, self-aligned contacts are usually produced. Via holes are thereby usually etched in a BPSG layer

deposited between the gate paths. Subsequently, these via holes are filled with a conductive material, so that a conductive connection is created.

The production of these via holes, however, becomes more and more difficult with ongoing structural miniaturization. In modern field effect transistors, a number of spacers are produced at or on the sidewalls of the gate webs, and these spacers, in interaction with suitable dopant implantations, see to it that the dopant profiles suitable for the respective purpose can be produced in the source/drain regions. Due to the spacers arranged between the gate paths and the demand that the via hole should be arranged between the spacers insofar as possible, the distance between the gate paths or, respectively, the diffusion region that serves the purpose of contacting must be selected adequately large, and this has a negative influence on the integration density that can be achieved.

When etching the via holes, the gate paths dare not be damaged, since a short would otherwise arise between the diffusion contact and the gate. Since, despite all efforts, one cannot prevent the gate paths from being attacked when etching the via holes, a thick protective layer, which was referred to as a "cap", is usually arranged on the gate paths, and this is intended to prevent a short between contact and gate. The relatively great thickness of this protective layer, however, deteriorates the quality of the gate paths and usually prevents a silicidization of the gate paths as well as the subsequent doping of the polysilicon of the gate paths (dual work function gate).

Due to the tight conditions between the gate paths, it is necessary that the insulation layer be subjected to a temperature treatment at relatively high temperatures in order to achieve a flowing of the insulation layer. Nonetheless, holes, what are referred to as voids, can occur between the gate paths during the deposition of the insulation layer. When the via holes are then formed, it can occur

that two via holes are connected to one another via a void. In the subsequent filling of the via holes with a conductive material, the voids are usually also filled, so that a short between two contacts can arise which possibly leads to the outage of the entire circuit.

SUMMARY OF THE INVENTION

It is therefore the object of the present invention to offer a method for producing an integrated semiconductor component that minimizes or, respectively, entirely avoids these problems.

Inventively, a method for producing an integrated semiconductor component is offered that comprises the following steps:

preparing a semiconductor substrate having at least one first region and at least one second region;

producing gate paths in the first and the second regions of the semiconductor substrate;

producing source/drain regions neighboring the gate paths and at least two spacers at the gate paths in the first region of the semiconductor substrate;

producing source/drain regions neighboring the gate paths in the second region of the semiconductor substrate; and

forming contacts to predetermined source/drain regions before all spacers have been produced in the first region of the semiconductor substrate.

Inventively, a method for producing an integrated semiconductor component is also offered and has the following steps:

preparing a semiconductor substrate having at least one first region and at least one second region;

producing gate paths in the first and the second regions of the semiconductor substrate;

producing source/drain regions neighboring the gate paths as well as at least two spaces at the gate paths in the first region of the semiconductor substrate;

producing source/drain regions neighboring the gate paths in the second region of the semiconductor substrate; and

preparing contacts to predetermined source/drain regions before all spacers in the first region of the semiconductor substrate have been produced.

The inventive methods have the advantage that integration density in the second region of the semiconductor substrate can be noticeably increased. As a result of the feature that the formation of the contacts to the source/drain regions is undertaken or, respectively, readied in the second region of the semiconductor substrate at a time at which all spacers have not yet been produced, no unnecessary spacer production occurs in the second region, and this results in saving the chip area. The saved area can, for example, be used in order to arrange the gate paths closer together in the second region. The spacers can thereby be employed as an aid for setting the desired dopant profiles and/or as lateral insulation of the gate paths.

In addition, the inventive methods can be integrated without difficulty in a process sequence that already exists for producing a semiconductor component. In particular, the process steps for the manufacture of a very fast logic circuits can be retained nearly unmodified. Problems which occurred with traditional methods due to the occurrence of voids between the transistors can be either clearly reduced or

entirely avoided given the inventive methods. Due to the early formation or, respectively, preparation of the contacts, high aspect ratios can be avoided and, as a result, the processes can be implemented more stably overall. The contacts can thereby also be already formed or, respectively, prepared at a time at which the source/drain regions have not yet been formed.

According to a preferred embodiment, landing pads are formed in the second region of the semiconductor substrate for preparing the contacts to predetermined source/drain regions. Doped polysilicon is preferably employed for forming the landing pads or, respectively, the contacts themselves.

According to another preferred embodiment, sacrificial contacts are formed in the second region of the semiconductor substrate for preparing the contacts to predetermined source/drain regions. The sacrificial contacts likewise prevent the production of unnecessary spacers on the gate paths in the second region of the semiconductor substrate. They are removed only when the actual contacts to the source/drain regions are formed.

According to a preferred embodiment, the spacers are formed of silicon oxide, silicon nitride or oxynitride. To that end, a silicon oxide layer, silicon nitride layer or oxynitride layer is deposited over the gate paths and etched back with an anisotropic etching, so that parts of these layers remain at the sidewalls of the gate paths. By employing these spacers, the dopings of the source/drain region can be set very precisely to correspond to the respective demands.

According to another preferred embodiment, the gate paths are formed in a polysilicon layer and a protective layer, particularly a silicon nitride layer, silicon oxide layer or oxynitride layer is produced and these layers are structured in common to form gate paths. It is thereby particularly preferred when the protective layer is produced with a thickness so that the protective layer comprises a thickness less than

100 nm, preferably in a range between 40 and 60 nm, after the gate structuring. This protective layer is frequently referred to as a "cap" and, in traditional processes, serves among other things as a hard mask for gate structuring and for protecting the gate paths during an etching process for producing the via holes. In the prior art, a dry-etching process that etches oxide selectively relative to the cap material must be utilized for this purpose. Since the structure to be etched exhibits a high aspect ratio in the prior art, the selectivity of the etching process is not very high, and a relatively thick "cap" must be employed in order to avoid a short between the gate path and the contact.

Since the formation of the contact is already undertaken or, respectively, prepared at a very early stage in the inventive methods, the "cap" now serves only for insulating the gate path from the contact and can therefore be selected relatively thin. Accordingly, the "cap" can be completely removed from the gate paths in the first region in later process steps, for example when etching a nitride spacer, and without additional process steps, this opens up the possibility of doping various gate paths with different dopants and thus constructing what are referred to as dual work function gates. In addition, the gate paths can be silicided in this way and, as a result of the silicidation, the resistance of the gate paths is clearly reduced.

It is also preferred when the gate paths in the first region of the semiconductor substrate are doped with dopants having different conductivity types. As a result of what is referred to as these dual work function gates, extremely high-performance logic circuits can be constructed. In this way, the supply voltage can also be reduced without incurring any losses in the switching speed.

For reducing the resistances of the gate paths, it is preferred when silicide layers are produced on the gate paths in the first region of the semiconductor

substrate. In particular, it is preferred when $CoSi_2$, $TaSi_2$, $TiSi_2$ or WSi_x is employed as silicide layers, and these silicide layers are produced by a salicide method.

The invention is explained in greater detail below with reference to the drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1-8 are cross-sectional views illustrating various steps of a method according to a first exemplary embodiment of the present invention;

Figs. 9-12 are cross-sectional views illustrating various steps of a method according to a second exemplary embodiment of the present invention; and

Figs. 13-18 are cross-sectional views illustrating various steps of a method according to a third exemplary embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Figures 1 through 8 show a method according to a first exemplary embodiment of the present invention. A thin silicon oxide layer was produced on a silicon substrate 1. This silicon oxide layer, that is not shown in Fig. 1, serves as a gate oxide during the further course of the method. Dependent on the application, silicon oxide layers of different thicknesses are employed in different regions of the silicon substrate. A polysilicon layer 2 is arranged on the silicon oxide layer. In this embodiment of the present invention, the polysilicon layer 2 was deposited as an undoped polysilicon layer and is subsequently doped with the assistance of a photo technique. A silicon nitride layer 3 is arranged above the polysilicon layer 2. The thickness of the silicon nitride layer 3 amounts to approximately 50 nm after the gate structuring. During the further course of the method, this layer serves as what is referred to as a "cap nitride".

Before producing the silicon oxide layer, a n-well 4 or, respectively, p-wells 5, 6 were produced in the silicon substrate. The individual wells are separated from one another by isolations 7. In the present example, these isolations 7 are fashioned as what are referred to as shallow trench isolations. The first region 8 of the silicon substrate 1 is arranged at the left side of Fig. 1. In this first region 8, the transistors from which the logic circuit is constructed are produced later. The second region 9 of the silicon substrate 1 is arranged at the right side of Fig. 1. In this second region 9, the transistors that serve as selection transistors in the memory cells are produced later. The structure produced by these steps is shown in Fig. 1.

Subsequently, the silicon nitride layer 3 and the polysilicon layer 2 are structured by a photo technique to form gate paths or tracks 10 in the first region 8 and gate paths 10' in the second region 9 (see Fig. 2). A re-oxidation of the gate oxide occurs in order to eliminate possible defects that occurred in the etching of the silicon nitride layer 3 and of the polysilicon layer 2. Phosphorous is now implanted into the silicon substrate with a photo technique for producing what are referred to as the source/drain regions 11 of the n-channel transistors. After this implantation, another silicon nitride layer is deposited and is structured with an anisotropic etching. First insulating spacers, what are referred to as spacers 12, are formed on the sidewalls of the gate paths 10 and 10' as a result of this etching. After producing the spacers 12, boron is implanted in the silicon substrate with a photo technique, so that the p-channel transistors can also be produced. Subsequently, a still further silicon nitride layer 13 is deposited. The structure formed by these steps is shown in Fig. 2.

The transistors that are produced in the second region 9 of the silicon substrate 1 serve as selection transistors in the memory cells. The capacitors of the memory cells, which are formed as trench capacitors in the present example, are not shown in the Figures for reasons of clarity. A high integration density arises

particularly in the second region 9 of the silicon substrate 1. In order to be able to achieve this high integration density, a resist mask 15 is produced that is opened at the locations at which the source/drain terminals, i.e. the terminals for the bit lines and the selection transistors, are later produced. The silicon nitride layer 13 in the opening 14 of the mask 15 is removed with an anisotropic etching, so that the source/drain regions 11 of the selection transistors are uncovered. The first region 8 of the silicon substrate 1 is protected by the resist mask 15 and thus experiences no modification (see Fig. 3). Subsequently, the resist mask 15 is removed and a further or additional polysilicon layer 16 is deposited (see Fig. 4). This polysilicon layer 16 is a doped polysilicon layer.

The polysilicon layer 16 is now structured with the assistance of a further or additional photo technique. The polysilicon layer 16 is completely removed from the first region 8 of the silicon substrate 1. The remaining part of the polysilicon layer 16 forms what is referred to as a "landing pad" 17 in the second region 9 of the silicon substrate, as shown in Fig. 5.

Subsequently, a still further silicon oxide layer is deposited. This silicon oxide layer is structured by a further anisotropic etching, so that a further spacer 18, which includes part of the silicon nitride layer 13 and the still further silicon oxide layer, arises on spacers 12 on the sidewalls of the gate paths 10 in the first region 8 of the silicon substrate. As a result of the sequence of these spacers 12 and 18 on the sidewalls of the gate paths 10 in the first region 8 of the silicon substrate and a suitably selected dopant implantations, the source/drain regions 11 of the transistors in the first region 8 can be set so that transistors having extremely short switching times can be produced. Accordingly, extremely high-performance logic circuits can be constructed. Due to the polysilicon layer 16, no deposition of the silicon oxide layer between the gate paths 10' of the selection transistors occurs in the second

region 9 of the silicon substrate. Accordingly, silicon oxide spacers 18 are also not produced between the gate paths 10' of the selection transistors. The area that is thereby saved between the gate paths 10' of the selection transistors can be used in order to arrange the gate paths correspondingly closer together, as a result whereof the integration density in the memory cell field is increased.

The remaining part of the silicon nitride layer 3 on the gate paths 10 in the first region 8 of the silicon substrate is removed with a further etching. This is possible because the silicon nitride layer 3 exhibits an extremely slight thickness in comparison to traditional methods. As a result of the removal of the silicon nitride layer 3, the gate paths 10 can now be doped in the desired type and fashion. A different doping of the various gate paths 10 is also possible in a simple way (dual work function gates). In this way, extremely fast logic circuits can be produced. The structure formed by these steps is shown in Fig. 6.

Subsequently, a silicide-forming metal, for example tantalum, titanium, tungsten or cobalt, is sputtered on. A silicide reaction occurs on the uncovered silicon regions as a result of a thermal treatment, namely the gate paths in the first region as well as the uncovered source/drain regions, whereas the silicide-forming metal is preserved essentially unmodified in the other regions and can thereby be removed in turn in a simple way. The results are selective and self-aligned silicide layers 19 (see Fig. 7) on the gate paths 10 in the first region 8 and the uncovered source/drain regions 11 ("salicide method"). The resistance of the gate paths 10 is clearly reduced by the silicide layers 19, and this has a positive influence on the performance capability of the logic circuit. In addition, the silicidation of the source/drain regions 11 clearly lowers the contact resistance, and this likewise has a positive influence on the performance capability of the logic circuit.

Subsequently, a thin silicon nitride layer is deposited, and this layer serves as barrier. For reasons of clarity, this thin silicon nitride layer is not shown. This is followed by the deposition of borophosilicate glass or BPSG layer 20 that is planarized by a chemical mechanical planarization or CMP step. A thermal treatment is implemented before the CMP step, so that the BPSG layer 20 can fill out the interspaces between the transistors as well as possible. The structure produced by these steps is shown in Fig. 7.

Via holes 21 are now produced in the BPSG layer 20 with a further photo technique, as shown in Fig. 8. These via holes 21 lead both to the silicon substrate 1 as well as to the gate paths 10. In the second region 9 of the silicon substrate, the via hole is conducted to the polysilicon layer 16 that serves as landing pad 17. After deposition of what is referred to as a liner (not shown), the via holes are filled with tungsten, and a CMP step is implemented in order to remove tungsten from the substrate surface outside the via holes.

For a complete production of the integrated circuit, the metalization as well as the passivation are subsequently constructed with a number of known steps. The inventive method has the advantage that the integration density in the second region of the semiconductor substrate can be clearly increased. Over and above this, the properties of the transistors in the first region of the semiconductor substrate can be clearly improved with little added outlay (silicidation, dual work function gates). The present invention, for example, therefore enables the cost-beneficial manufacture of what are referred to as embedded DRAM products.

Figs. 9 through 12 show a method according to a second exemplary embodiment of the present invention. The first steps of this method thereby agree with the steps shown in Figs. 1 through 4 and shall therefore not be repeated here.

In contrast to the first exemplary embodiment of the present invention, a relatively thick polysilicon layer is deposited. The polysilicon layer is structured with the assistance of a further photo technique. The polysilicon layer is thereby again completely removed from the first region 8 of the silicon substrate. The remaining part of the polysilicon layer forms the complete contact 24 in the second region 9 of the silicon substrate, as shown in Fig. 9.

A further silicon oxide layer is subsequently deposited. This silicon oxide layer is structured by a further anisotropic etching so that a further spacer 18, which comprises part of the silicon nitride layer 13 and the silicon oxide layer, is formed on the spaces 12 on the sidewalls of the gate paths 10 in the first region 8 of the silicon substrate. Due to the contact 24, no deposition of the silicon oxide layer occurs in the second region 9 of the silicon substrate between the gate paths 10' of the selection transistors. Accordingly, silicon oxide spacers 18 are also not produced between the gate paths 10' of the selection transistors. The area, that is thereby saved between the gate paths 10' of the selection transistors, can be utilized in order to arrange the gate paths 10' correspondingly closer together, as a result whereof the integration density in the memory cell field is increased.

The remaining parts of the silicon nitride layer 3 on the gate paths 10 in the first region 8 as well as partly on the paths 10' in the second region 9 of the silicon substrate are removed with a further etching. This is possible because the silicon nitride layer 3 exhibits a very slight thickness compared to traditional methods. As a result of the removal of the silicon nitride layer 3, the gate paths 10 and 10' can now be doped in the desired way and fashion. A different doping of the various gate paths 10 and 10' is also possible in a simple way (dual work function gates). Very fast logic circuits can be produced in this way. The structure formed by these steps is show in Fig. 10.

Subsequently, a silicide forming metal, for example tantalum, titanium, tungsten or cobalt is sputtered on (see Fig. 11). As a result of a thermal treatment, a silicide reaction occurs on the uncovered silicon regions, namely the gate paths 10 and 10' as well as the uncovered source/drain regions 11, whereas the silicide-forming metal remains essentially unmodified in the other regions and can therefore be simply removed in turn. The result are selective and self-aligned silicide layers 19 on the gate paths 10 and 10' and the uncovered source/drain regions 11 ("salicide method"). As a result of the silicide layers 19, the resistance of the gate paths 10 and 10' is clearly reduced, and this has a positive effect on the performance capability of the logic circuit as well as of the word lines in the cell field. In addition, the contact resistance is clearly reduced due to the silicidation of the source/drain regions 11, and this likewise has a positive influence on the performance capability of the logic circuit.

Subsequently, a thin silicon nitride layer is deposited, and this serves as barrier. For reasons of clarity, this thin silicon nitride layer is not shown. This is followed by the deposition of a BPSG layer 20 (see Fig. 11) that is subjected to a thermal treatment so that the BPSG layer 20 can fill out the interspaces between the transistors as well as possible. Subsequently, the BPSG layer 20 is planarized with a CMP step. The CMP step is implemented so that the contact 24 is uncovered. Only the first metallization layer therefore need be deposited in order to produce a conductive connection to the source/drain regions of the selection transistors in the memory cell field. This structure is shown in Fig. 11.

Via holes 21 are now produced in the BPSG layer 20 with a further or additional photo technique. These via holes 21 lead both to the silicon substrate of the remaining transistors as well as to the gate paths 10. After deposition of what is referred to as a liner (not shown), the via holes are filled with tungsten and a CMP

step is implemented in order to remove tungsten from the substrate surface outside the via holes 21. The structure which is produced by these steps is shown in Fig. 12.

For complete manufacture of the integrated circuit, the metallization as well as the passivation are built up again with a number of known steps. This inventive method also has the advantage that the integration density in the second region of the semiconductor substrate can be clearly increased. Over and above this, the properties of the transistors in the first region 8 of the semiconductor substrate can be clearly improved with a slight added outlay (silicidation, dual work function gates).

Figures 13 through 18 show a method according to a third exemplary embodiment of the present invention. In contrast to the first exemplary embodiment of the present invention, however, the polysilicon layer does not serve as a landing pad but what is referred to as a sacrificial contact.

A thin silicon oxide layer is produced on a silicon substrate 1. This silicon oxide layer, which is not shown in Figure 13, serves as gate oxide during the further course of the method. A polysilicon layer 2 is arranged on the silicon oxide layer. In this embodiment of the present invention, the polysilicon layer 2 was deposited as an undoped polysilicon layer and is subsequently doped with the assistance of a photo technique. A silicon nitride layer 3 is arranged over the polysilicon layer 2. The thickness of the silicon nitride layer 3 amounts to approximately 50 nm.

Before producing the silicon oxide layer, an n-well 4 or, respectively, p-wells 5, 6 are produced in the silicon substrate. The individual wells are thereby separated from one another by isolations 7. These isolations 7 are formed as what are referred to as shallow trench isolations in the present example. The silicon substrate is again divided into a first region 8 and into a second region 9, as shown in Fig. 13.

Subsequently, the silicon nitride layer 3 and the polysilicon layer 2 are structured with a photo technique to form gate paths 10 in the first region 8 and gate paths 10' in the second region 9. A re-oxidation of the gate oxide follows in order to eliminate possible defects that occurred in the etching of the silicon nitride layer 3 and of the polysilicon layer 2. Phosphorous is now implanted in the silicon substrate with a photo technique in order to produce what are referred to as source/drain regions 11 of the n-channel transistors. A further silicon nitride layer is deposited after this implantation and is structured with an anisotropic etching. First insulating spacers 12 are formed on the sidewalls of the gate paths 10 as a result of this etching. After producing the spacers 12, boron is implanted into the silicon substrate with a photo technique, so that the p-channel transistors can also be produced. Subsequently, a further silicon nitride layer 13 is deposited. The structure which is formed by these steps is shown in Figure 14.

A further polysilicon layer 16 is subsequently deposited, as shown in Fig. 15. This polysilicon layer 16 is an undoped polysilicon layer that later forms the sacrificial contact.

The polysilicon layer 16 is now structured with the assistance of a further photo technique. The polysilicon layer 16 is thereby completely removed from the first region 8 of the silicon substrate 1. The remaining part of the polysilicon layer 16 forms the sacrificial contact 25 in the second region 9 of the silicon substrate, as shown in Fig. 16.

A further silicon oxide layer is subsequently deposited. This silicon oxide layer is structured with a further anisotropic etching so that further spacers 18, which are made up of part of the layer 13 and the silicon oxide layers are formed on the spacers 12 on the sidewalls of the gate paths 10 in the first region 8 of the silicon substrate. Due to the sequence of these spacers 12 and 18 on the sidewalls of the gate

paths 10 in the first region 8 of the silicon substrate and a suitably selected dopant implantations, the source/drain regions 11 of the transistors in the first region 8 can be set so that transistors having extremely short switching times can be produced. Accordingly, extremely high-performance logic circuits can be constructed. Due to the sacrificial contact 25, no deposition of the silicon oxide layer occurs between the gate paths 10' of the selection transistors in the second region 9 of the silicon substrate. Accordingly, silicon oxide spacers 18 are also not produced between the gate paths 10' of the selection transistors. The area between the gate paths 10' of the selection transistors that is saved can be used in order to arrange the gate paths correspondingly closer together, so that the integration density in the memory cell field is increased as a result thereof.

The remaining part of the silicon nitride layer 3 on the gate paths 10 in the first region 8 of the silicon substrate is also removed with a further etching. This is possible because the silicon nitride layer 3 exhibits an extremely slight thickness compared to traditional methods. The gate paths 10 can now be doped in the desired way and fashion as a result of the removal of the silicon nitride layer 3. Subsequently, a silicide-forming metal, for example tantalum, titanium, tungsten or cobalt, is sputtered on. As a result of a thermal treatment, a silicide reaction occurs on the uncovered silicon regions, namely the gate paths 10 in the first region 8 as well as the uncovered source/drain regions 11, whereas the silicide-forming metal remains essentially unmodified in the other regions and can thereby be removed in turn in a simple way. The result are selective and self-aligned silicide layers 19 on the gate paths 10 in the first region and the uncovered source/drain regions 11 ("salicide method").

The deposition of a BPSG layer 20 follows and is planarized with a CMP step. A thermal treatment is implemented before the CMP step so that the BPSG

layer 20 can fill up the interspaces between the transistors as well as possible. The structure which is formed by these steps is shown in Fig. 17.

Via holes 21 are now produced in the BPSG layer 20 with a further photo technique. These via holes 21 lead both to the silicon substrate as well as to the gate paths 10 in the first region 8. The via hole is conducted to the sacrificial contact 25 in the second region 9 of the silicon substrate. A part of the sacrificial contact 25 and the silicon nitride layer 13 that still remains is removed with a dry-chemical or wet-chemical etching, so that there is now a space for the actual contact. This etching of the sacrificial contact 25 can be implemented with high selectivity relative to the surrounding material.

A deposition of what is referred to as a liner (not shown) and the deposition of a tungsten layer that serves the purpose of filling up the via holes 21 again occurs. In a further CMP step, the tungsten that is located outside the via holes is removed from the substrate surface. The structure which is formed by these steps is shown in Figure 18.

Due to the employment of the sacrificial contact 25, masking and etching steps can be eliminated compared to the first embodiment because the silicon nitride 13 need not be removed between selection transistors in the second region 9.

WE CLAIM:

Patent Claims

1. Method for producing an integrated semiconductor component comprising the steps:

a) a semiconductor substrate having at least one first region and at least one second region is prepared;

b) gate paths are produced in the first and in the second region of the semiconductor substrate;

c) source/drain regions neighboring the gate paths and at least two spacers at the gate paths are produced in the first region of the semiconductor substrate;

d) source/drain regions are produced neighboring the gate paths in the second region of the semiconductor substrate, and, for preparing the contacts to predetermined source/drain regions in the second region of the semiconductor substrate, sacrificial contacts are formed before all spacers have been produced in the first region of the semiconductor substrate.

2. Method according to claim 1, characterized in that the spacers are formed of silicon oxide, silicon nitride or oxynitride.

3. Method according to claim 1 or 2, characterized in that the gate paths are formed in that a polysilicon layer and a protective layer, particularly a silicon nitride, silicon oxide or oxynitride layer, are generated and these layers are structured in common to form gate paths.

4. Method according to claim 3, characterized in that the protective layer is generated with a thickness such that the protective layer exhibits a thickness of less than 100 nm after the gate structuring.

5. Method according to one of the preceding claims, the gate paths in the first region of the semiconductor substrate are doped with dopants having different conductivity types.

6. Method according to one of the preceding claims, characterized in that silicide layers are generated on the gate paths in the first region of the semiconductor substrate.

7. Method according to claim 6, characterized in that $CoSi_2$, $TaSi_2$, $TiSi_2$ or WSi_x are employed as silicide layers.

8. Method according to claim 6 or 7, characterized in that the silicide layers are produced with a salicide method.

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**IN THE UNITED STATES ELECTED OFFICE OF
THE UNITED STATES PATENT AND TRADEMARK OFFICE
UNDER THE PATENT COOPERATION TREATY - CHAPTER II**

SUBMISSION OF PROPOSED DRAWING CHANGES

APPLICANTS: Lars-Peter Heineck, Tobias Jacobs and Josef Winnerl

ATTORNEY DOCKET NO.: P02,0022

SERIAL NO.: EXAMINER:

FILING DATE: ART UNIT:

INTERNATIONAL APPLICATION NO.: PCT/DE99/02339

INTERNATIONAL FILING DATE: 29 July 1999

INVENTION: "METHOD FOR PRODUCING INTEGRATED SEMICONDUCTOR COMPONENTS"

BOX PCT
Assistant Commissioner for Patents
Washington, D.C. 20231

S I R:

Applicants propose to make changes to Figs. 2-18, which changes are indicated in red in the attached drawings and include the addition of element numbers and changing the element number 10 in the area 9 to be 10'.

If these corrections are approved by the Examiner, Formal Drawings incorporating these changes will be submitted once the application has been allowed.

Respectfully submitted,

(Reg. No. 24,149)

James D. Hobart
SCHIFF HARDIN & WAITE
Patent Department
6600 Sears Tower
233 South Wacker Drive
Chicago, Illinois 60606
Telephone: (312) 258-5781
Customer Number 26574

DATED: January 28, 2002

FIG 1

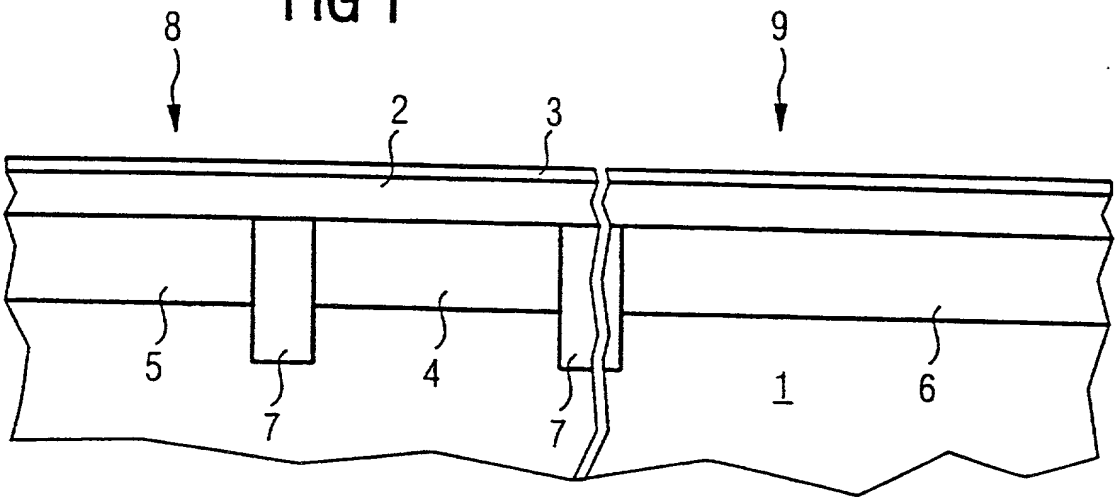

FIG 2

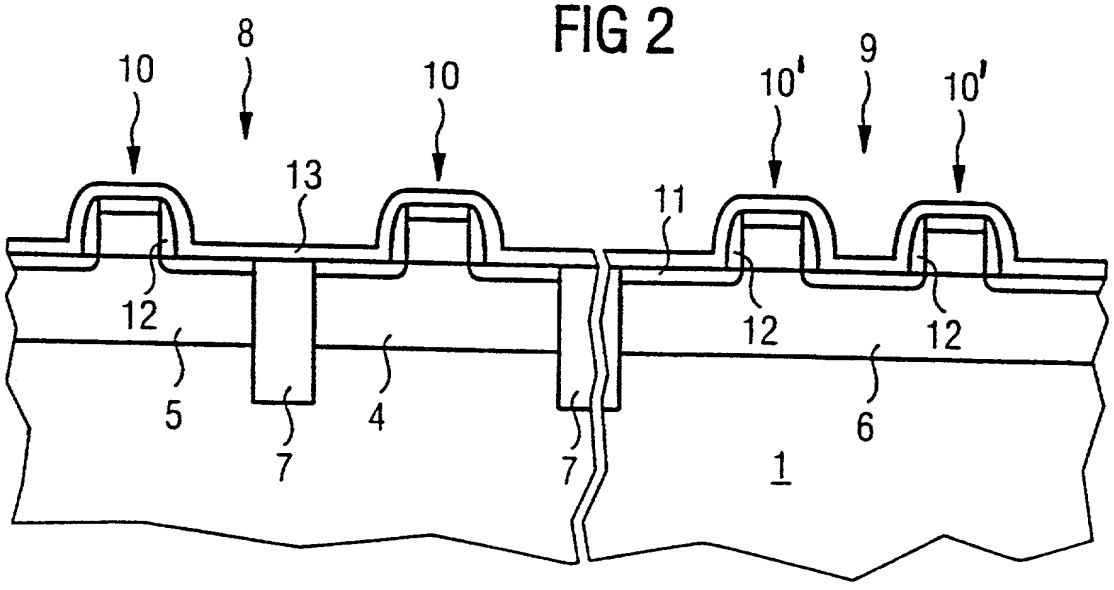

FIG 3

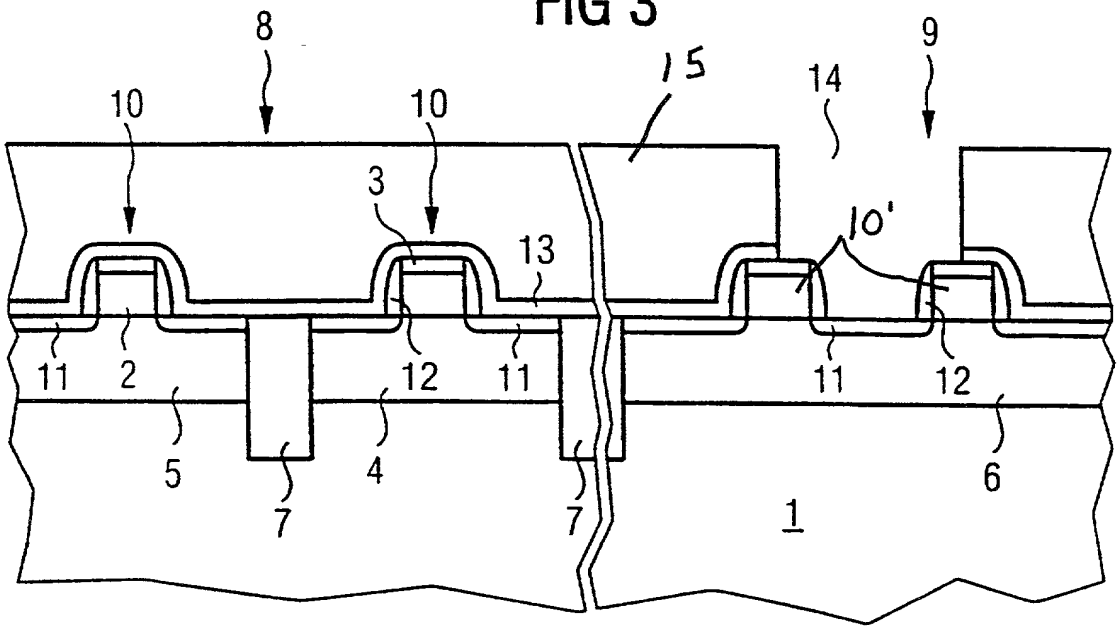
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FIG 4

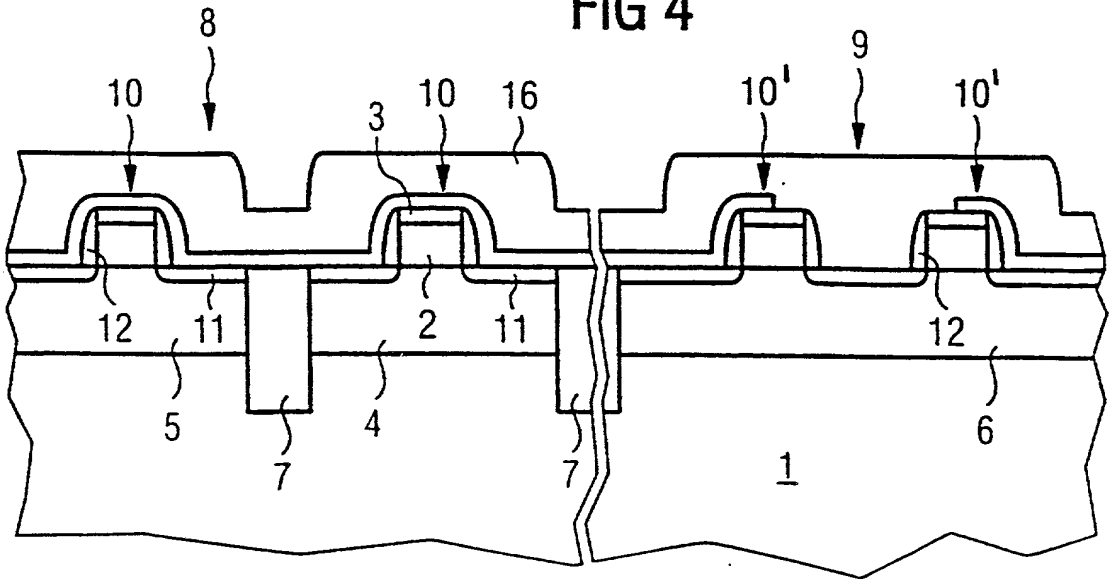
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FIG 5

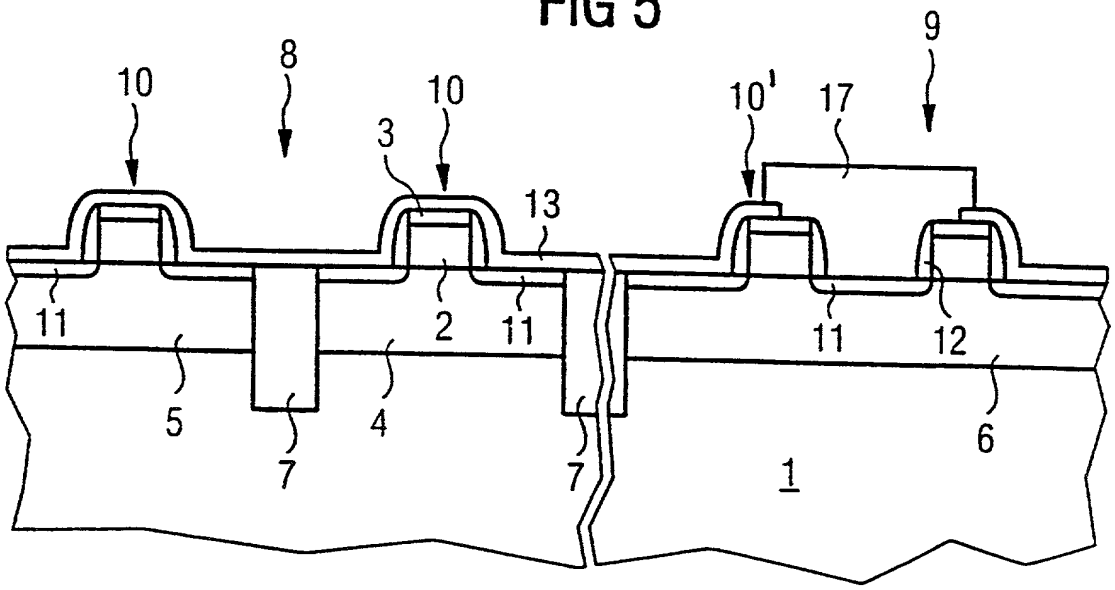
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FIG 6

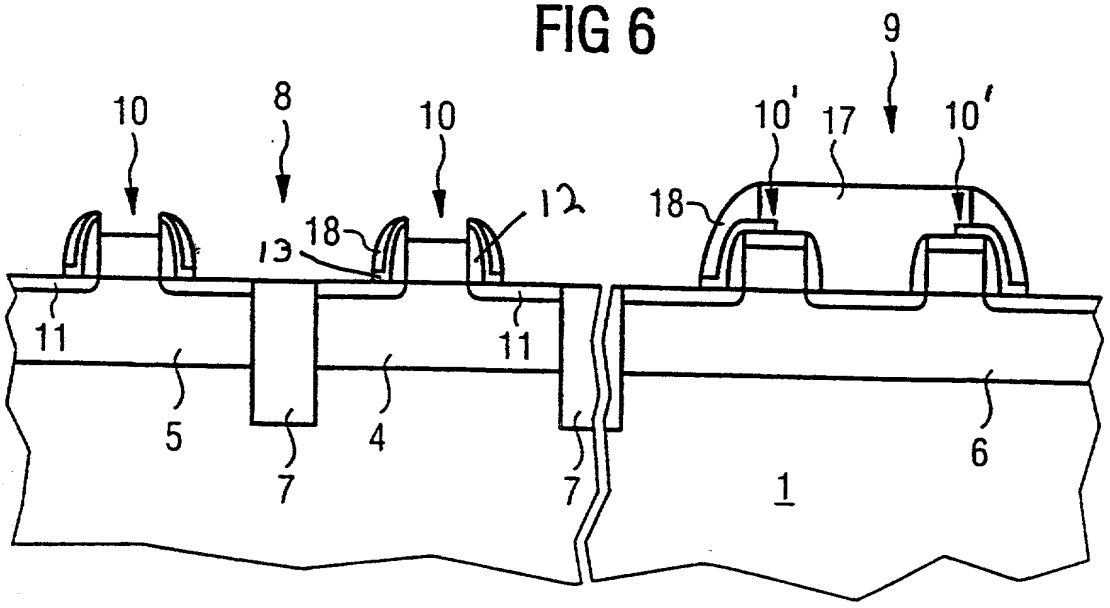
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FIG 7

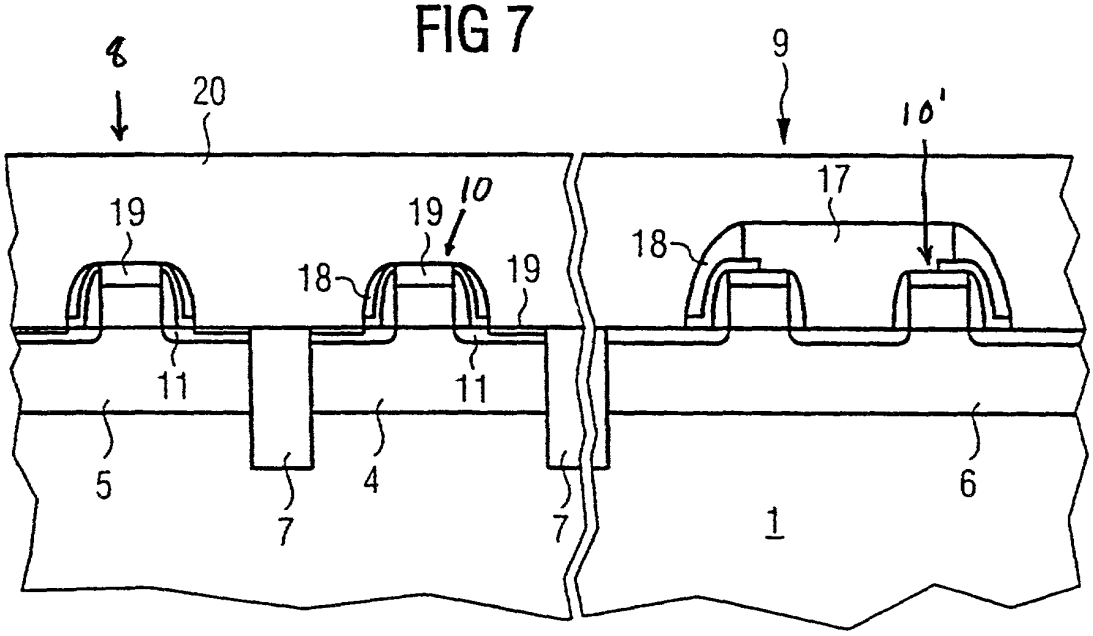

FIG 8

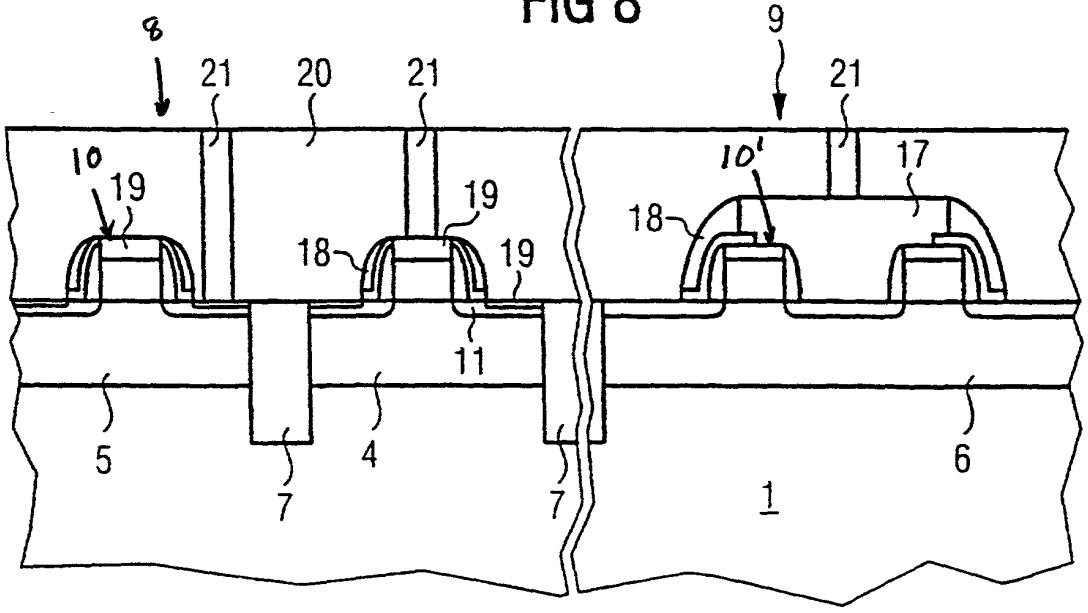

FIG 9

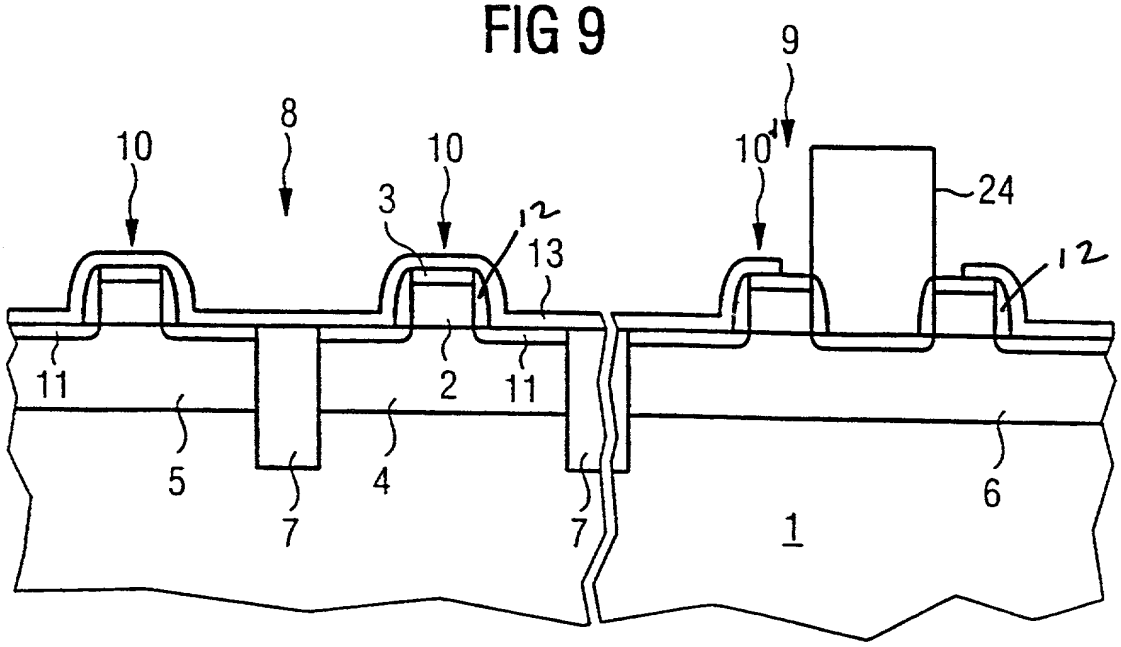
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FIG 10

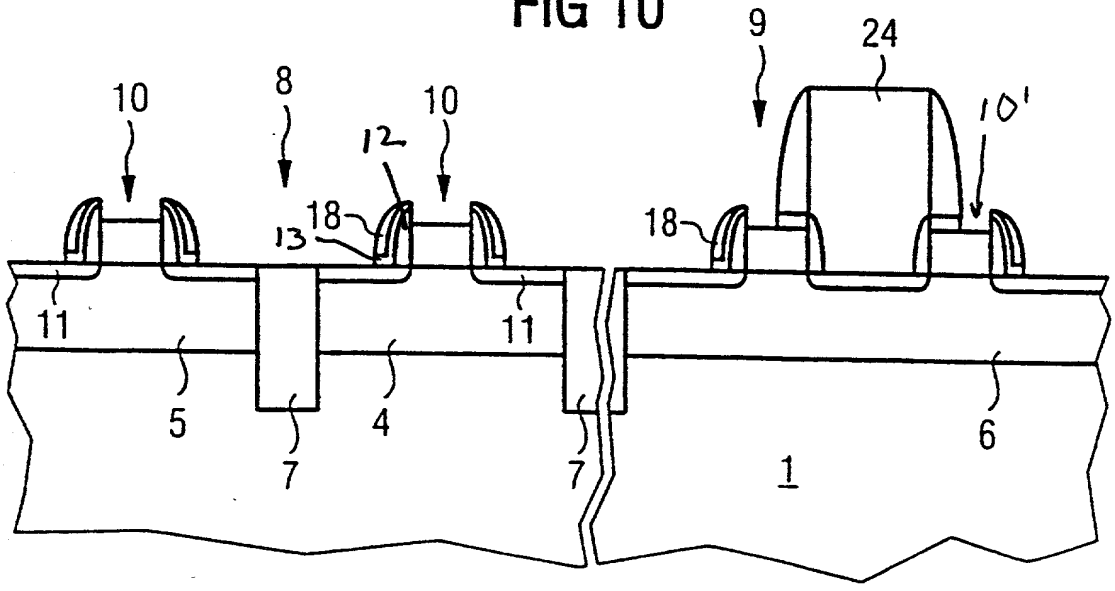
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FIG 11

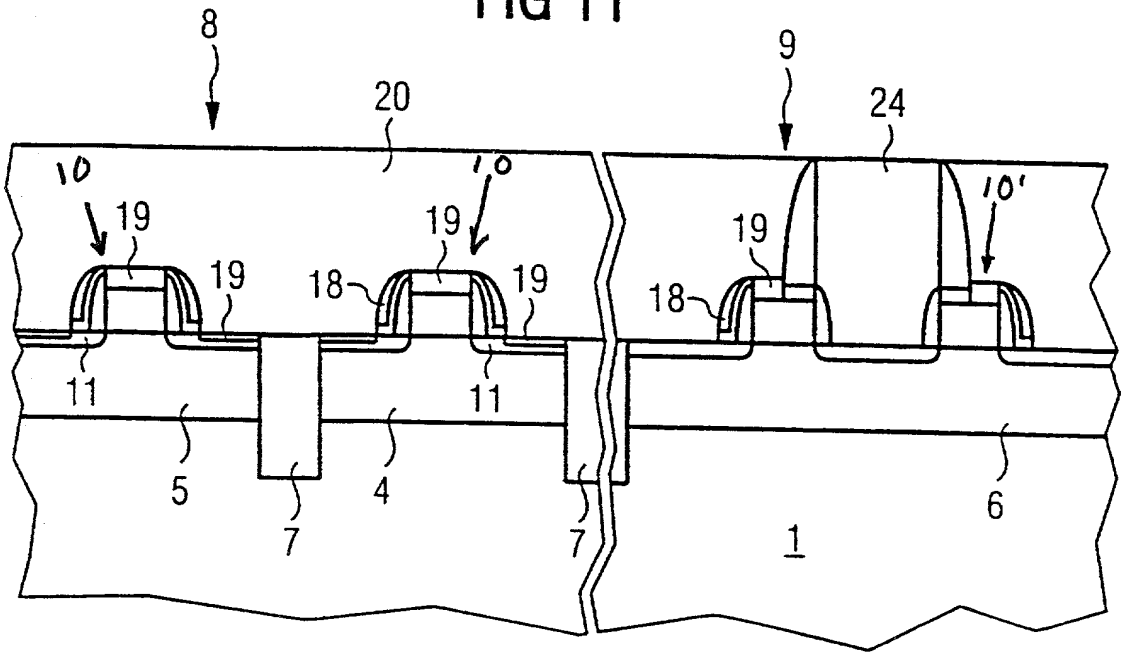
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FIG 12

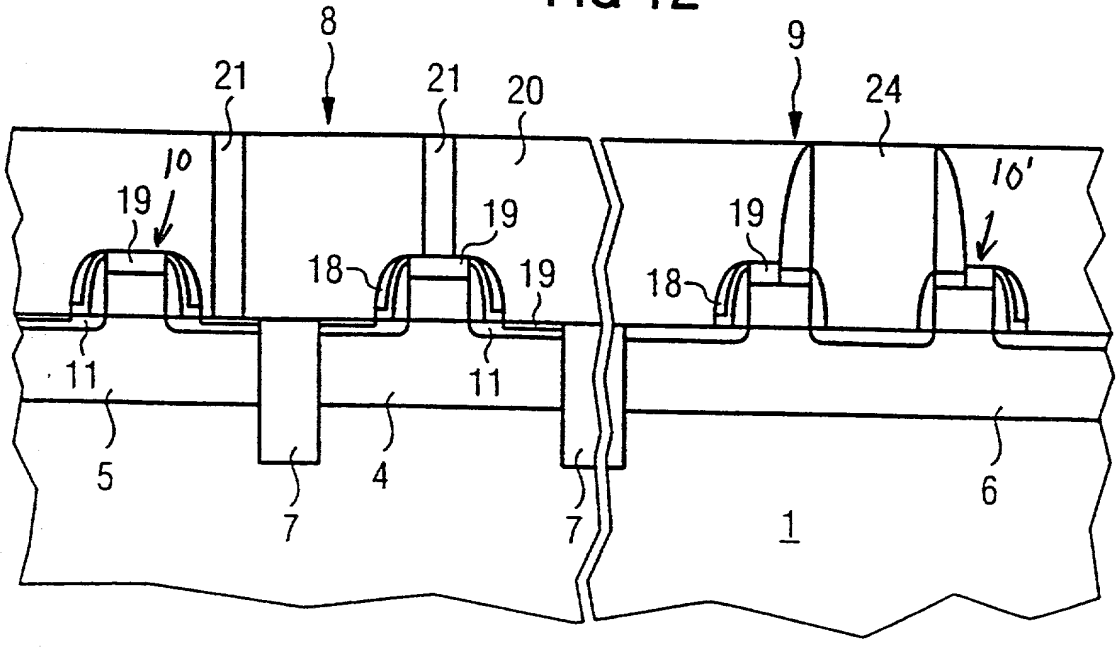
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FIG 13

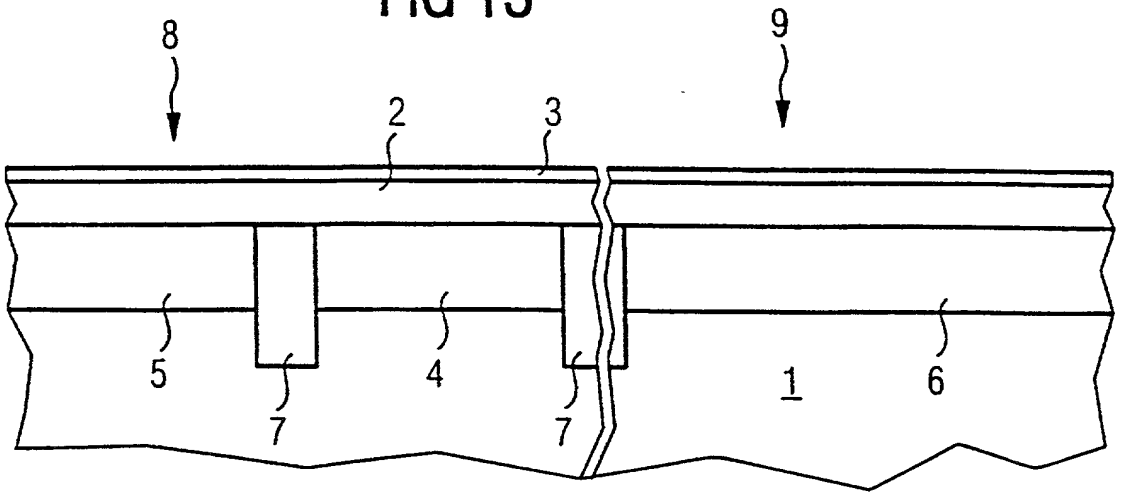

FIG 14

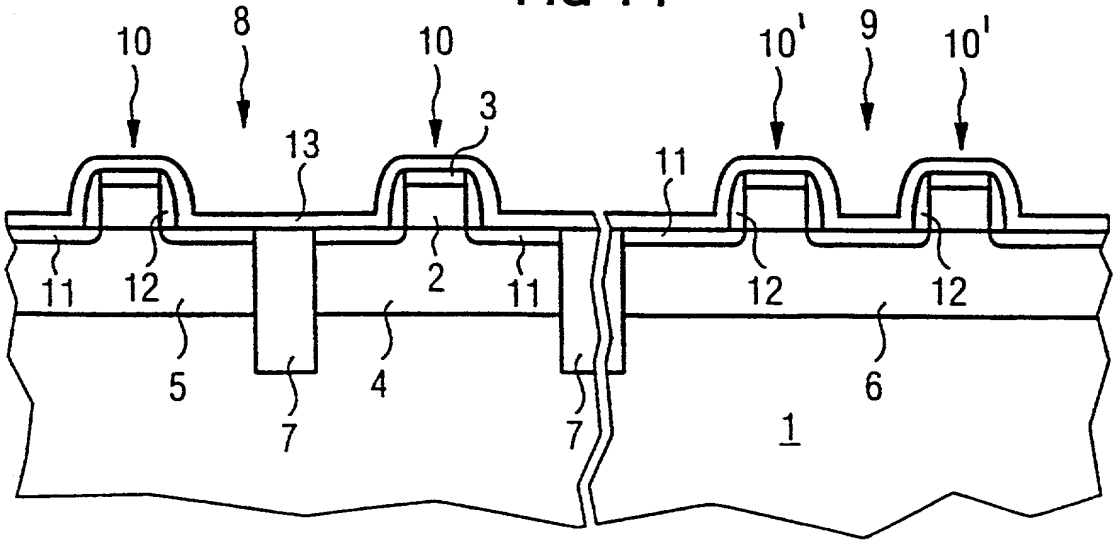

FIG 15

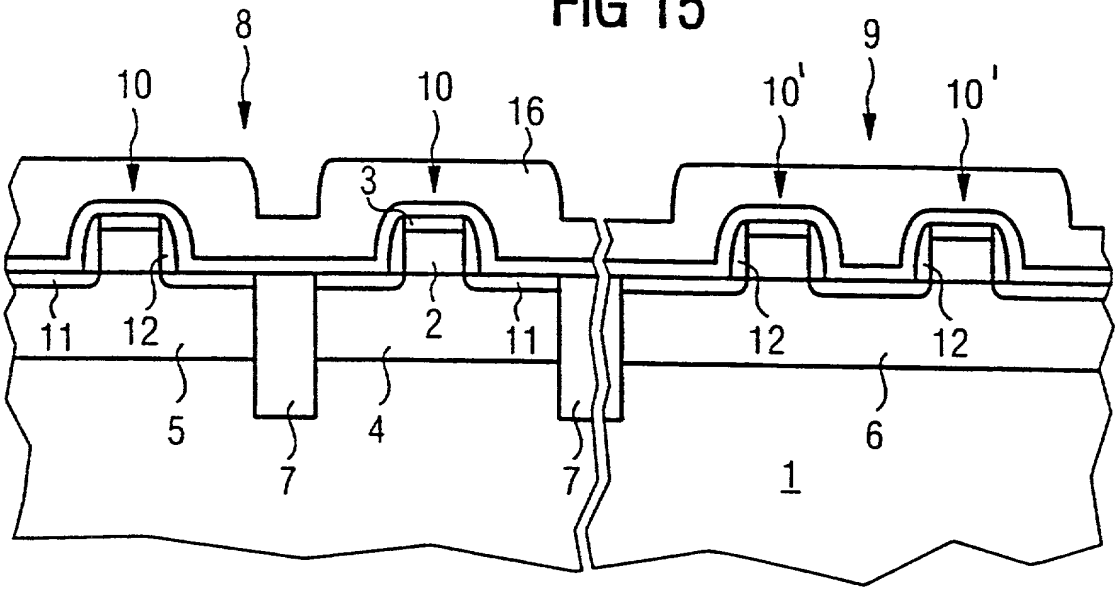
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FIG 16

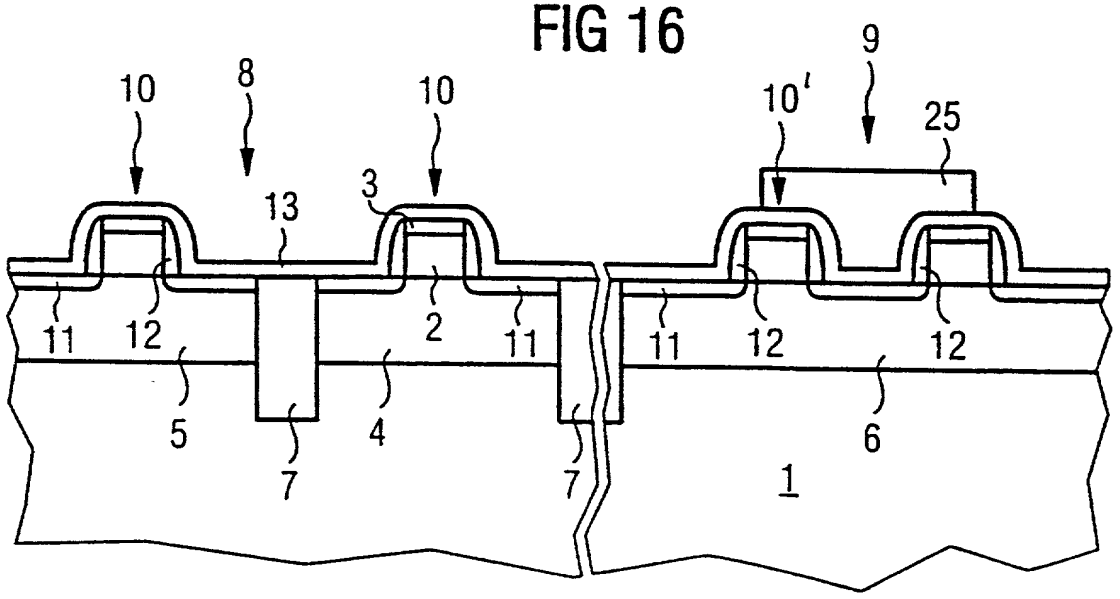
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FIG 17

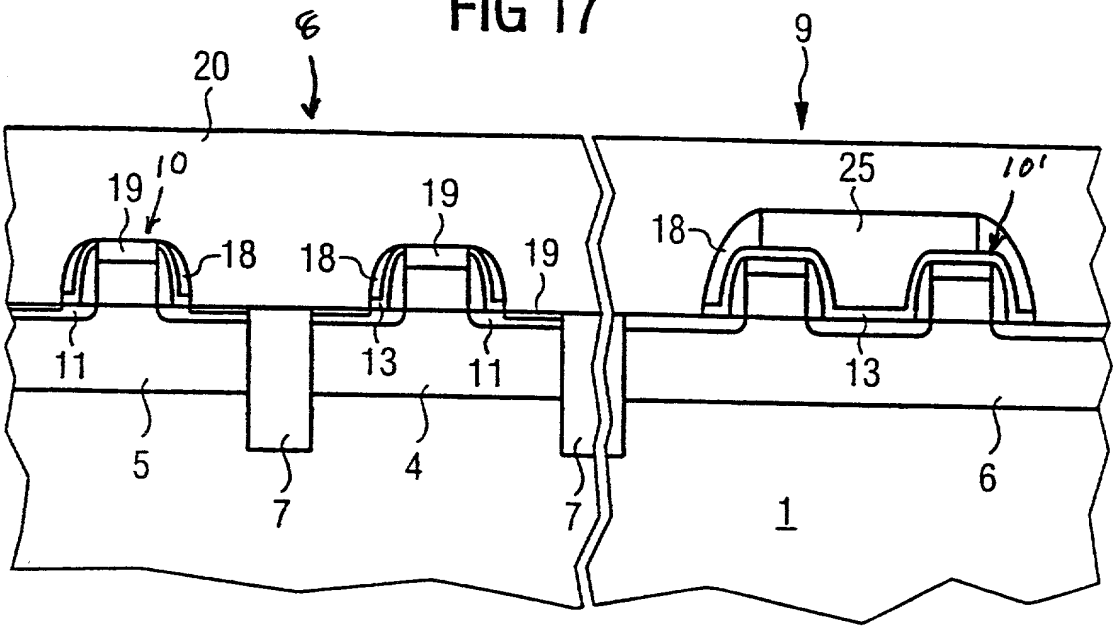
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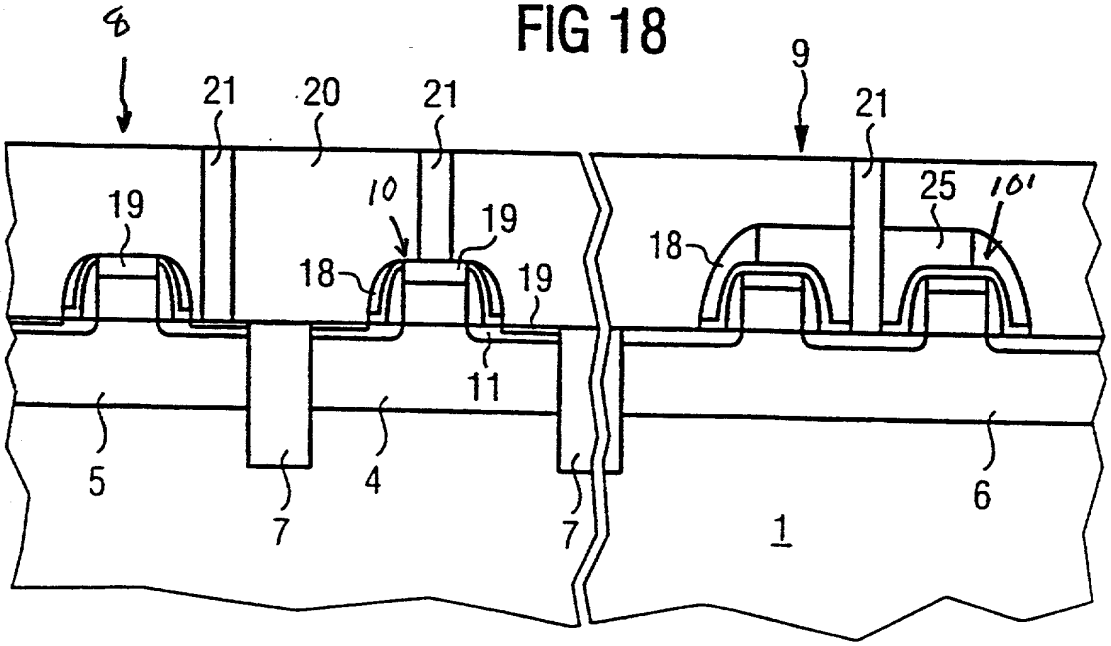
FIG 18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**IN THE UNITED STATES ELECTED OFFICE OF
THE UNITED STATES PATENT AND TRADEMARK OFFICE
UNDER THE PATENT COOPERATION TREATY - CHAPTER II**

SUBMISSION OF DRAWINGS

APPLICANTS: Lars-Peter Heineck, Tobias Jacobs and Josef Winnerl

ATTORNEY DOCKET NO.: P02,0022

SERIAL NO.: EXAMINER:

FILING DATE: ART UNIT:

INTERNATIONAL APPLICATION NO.: PCT/DE99/02339

INTERNATIONAL FILING DATE: 29 July 1999

INVENTION: "METHOD FOR PRODUCING INTEGRATED SEMICONDUCTOR COMPONENTS"

BOX PCT
Assistant Commissioner for Patents
Washington, D.C. 20231

S I R:

Attached herewith are nine sheets of Formal Drawings containing Figs. 1-18.

Respectfully submitted,

(Reg. No. 24,149)

James D. Hobart
SCHIFF HARDIN & WAITE
Patent Department
6600 Sears Tower
233 South Wacker Drive
Chicago, Illinois 60606
Telephone: (312) 258-5781
Customer Number 26574

DATED: January 28, 2002

WO 01/09946 PCT/DE99/02339

FIG 1

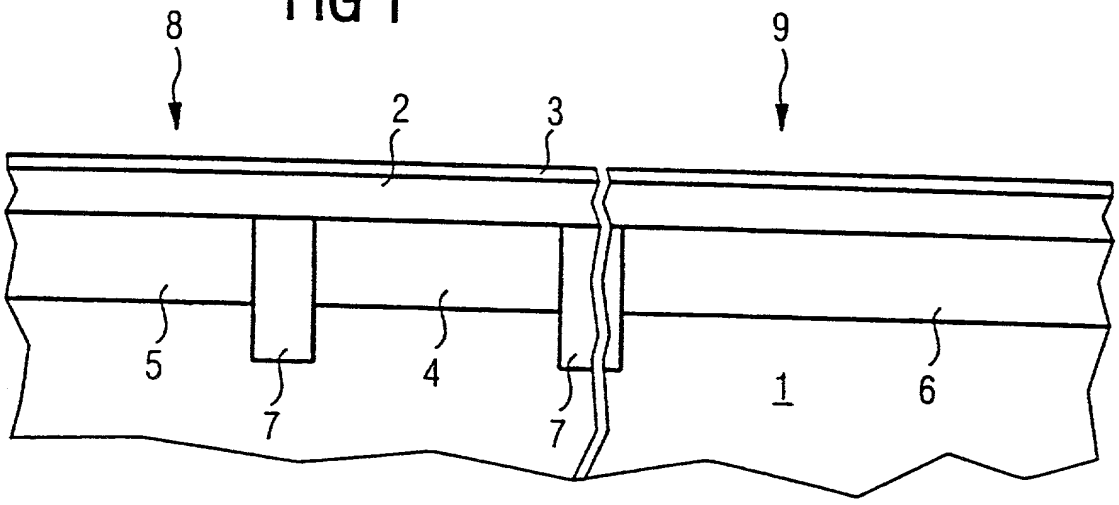

FIG 2

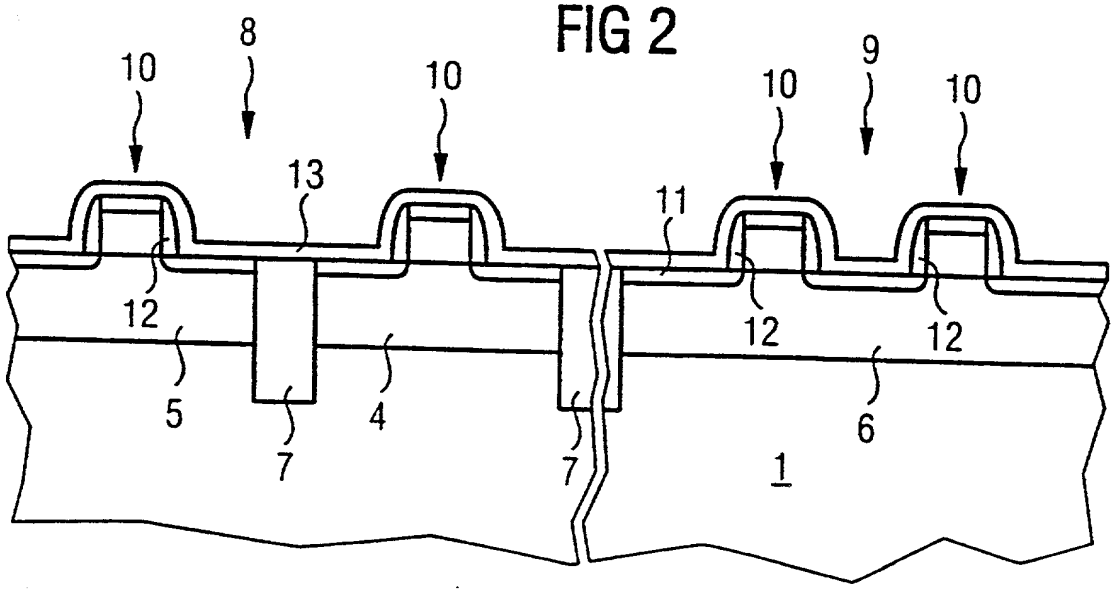

FIG 3

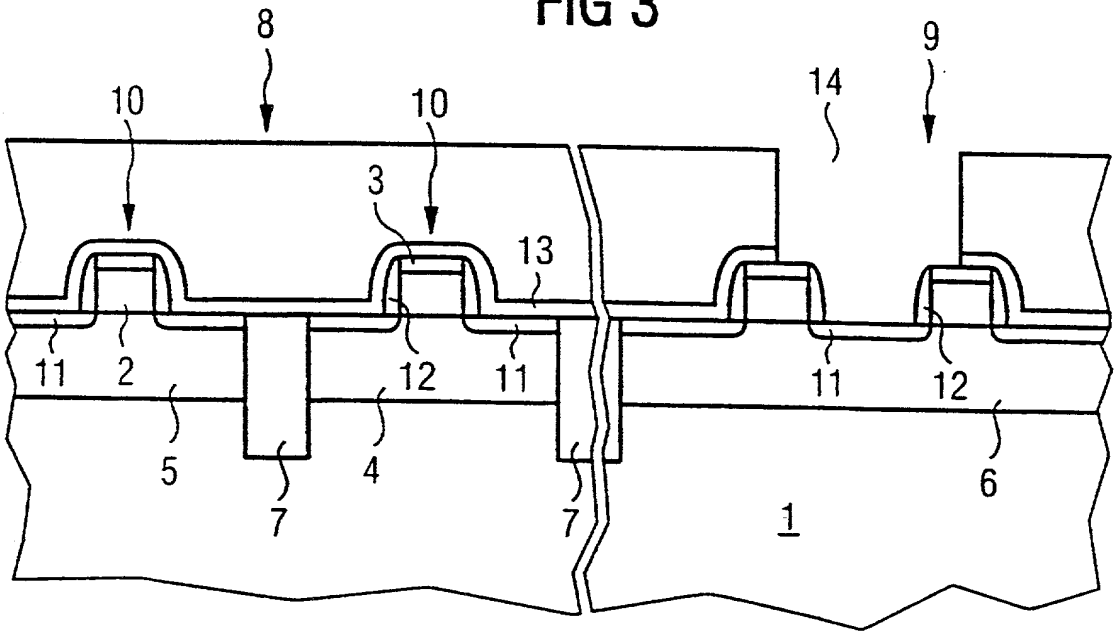
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FIG 4

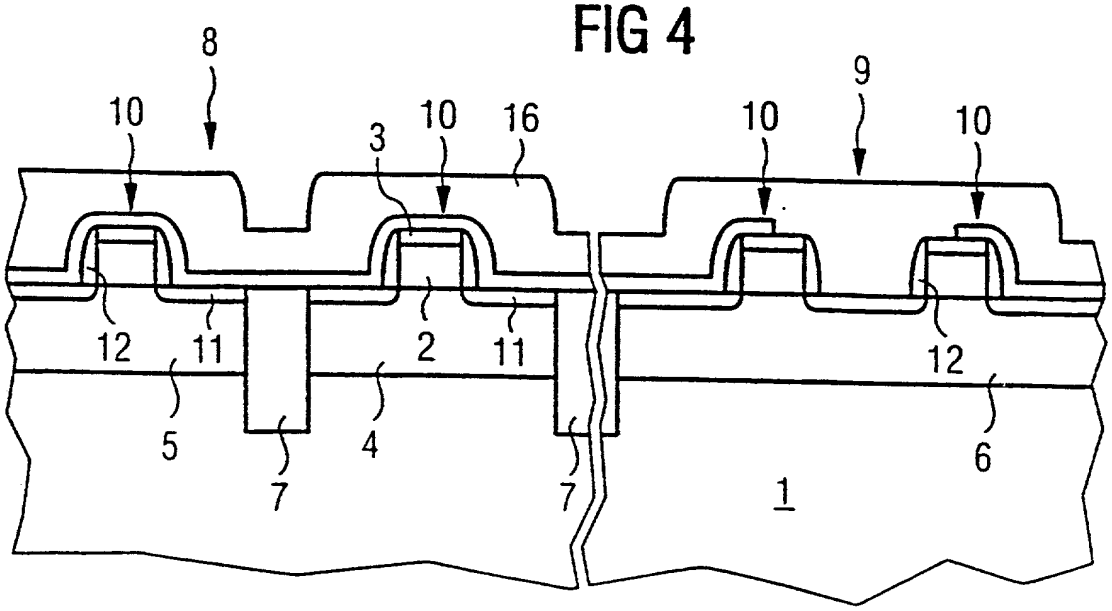
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FIG 5

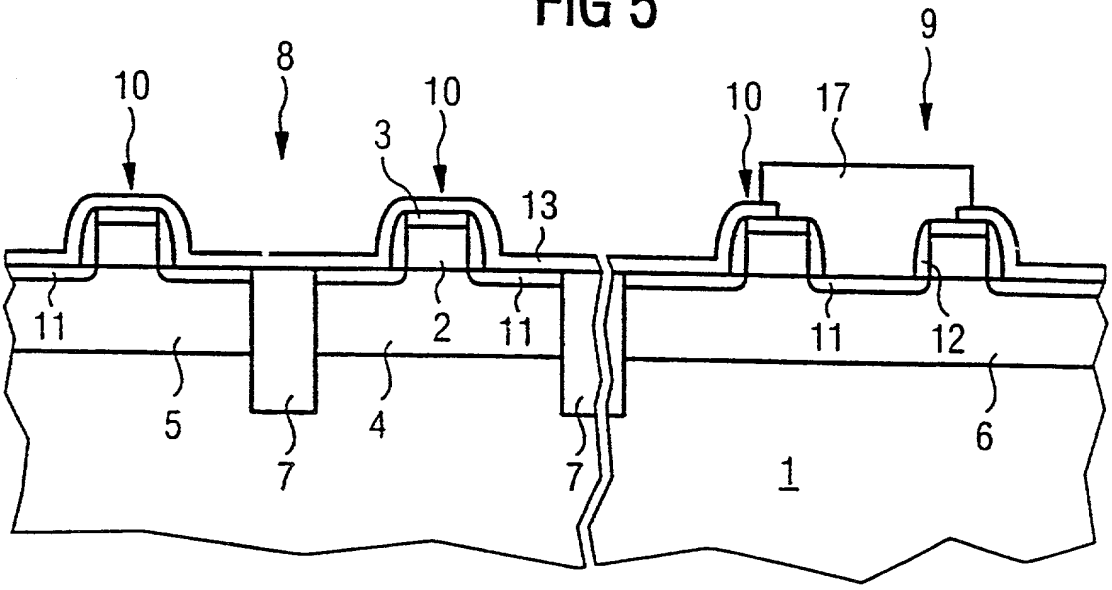
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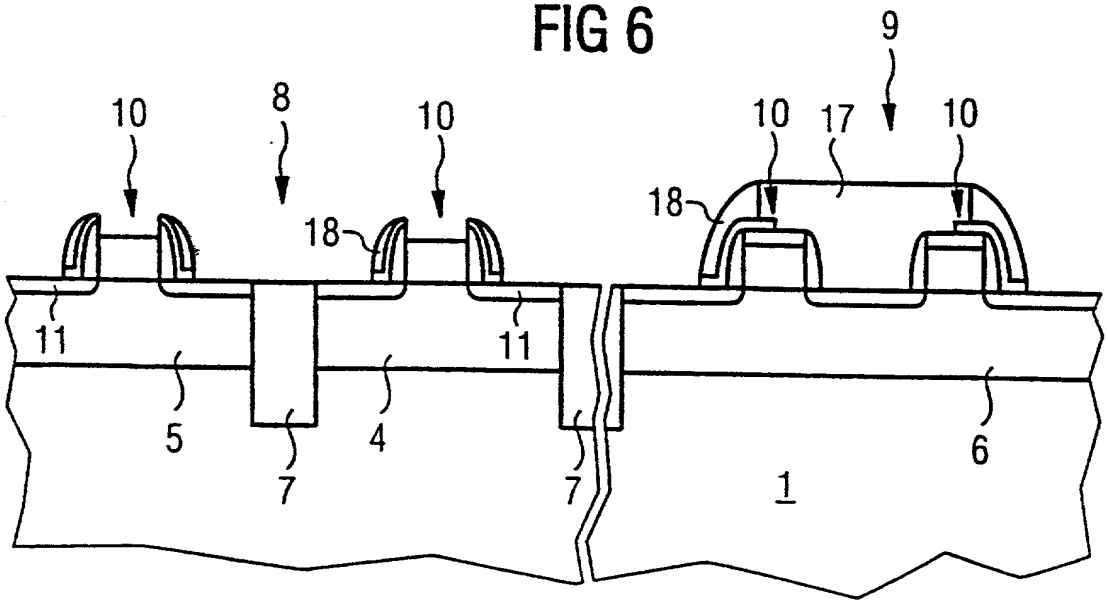
FIG 6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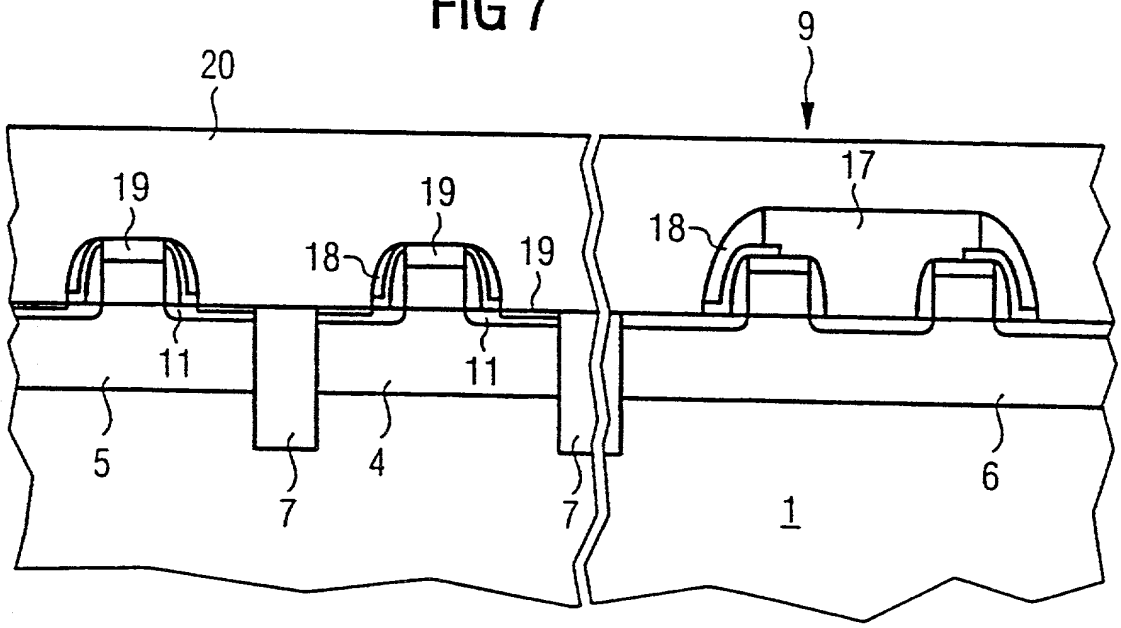
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FIG 8

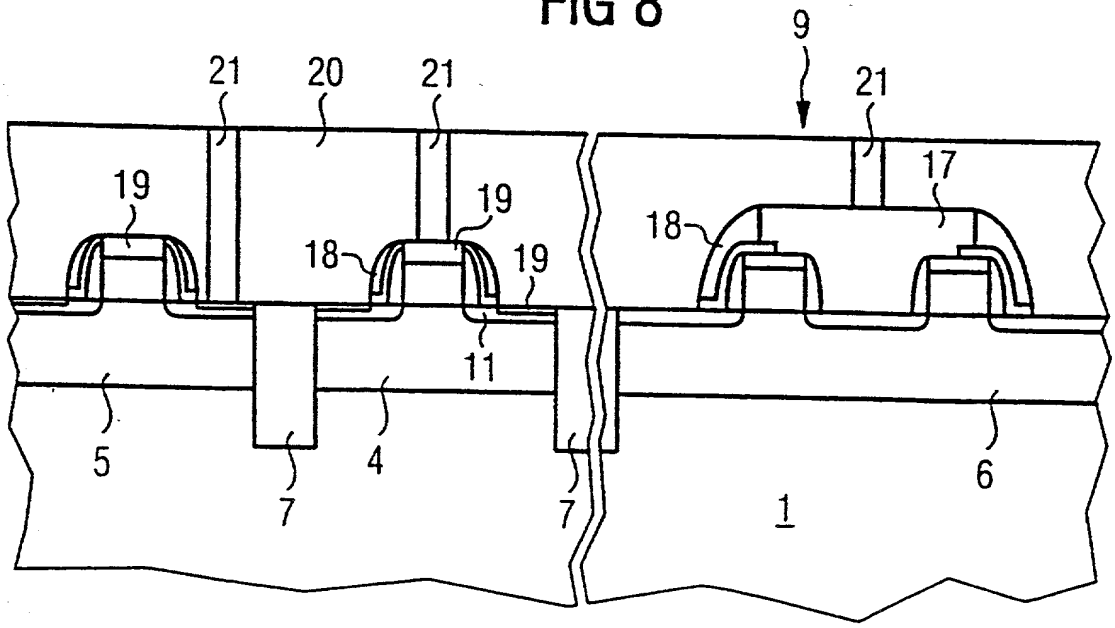
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FIG 9

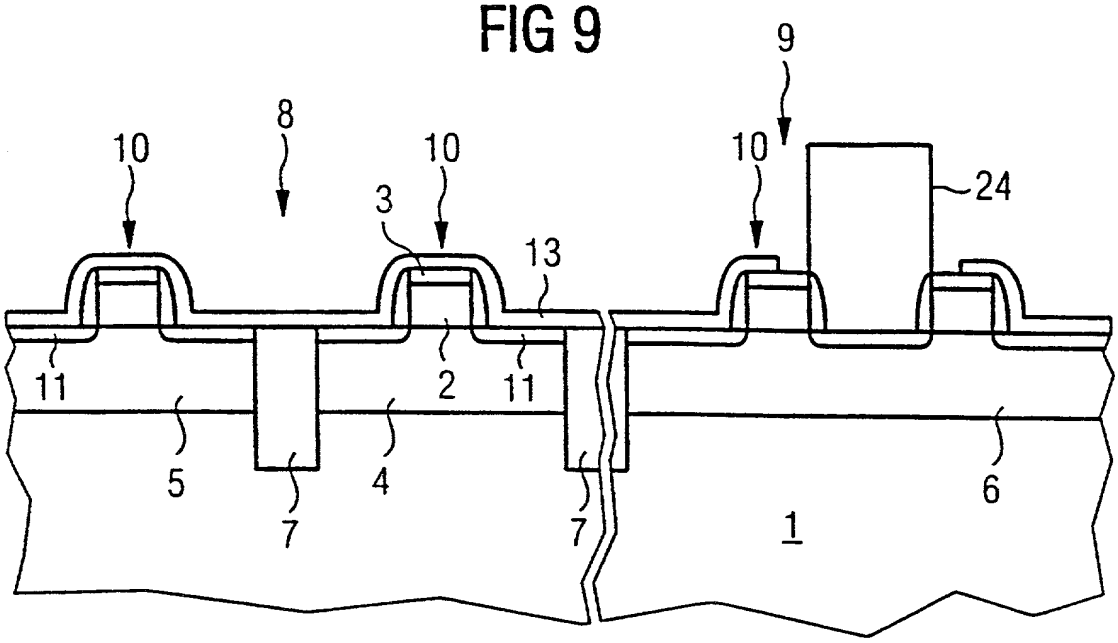

FIG 10

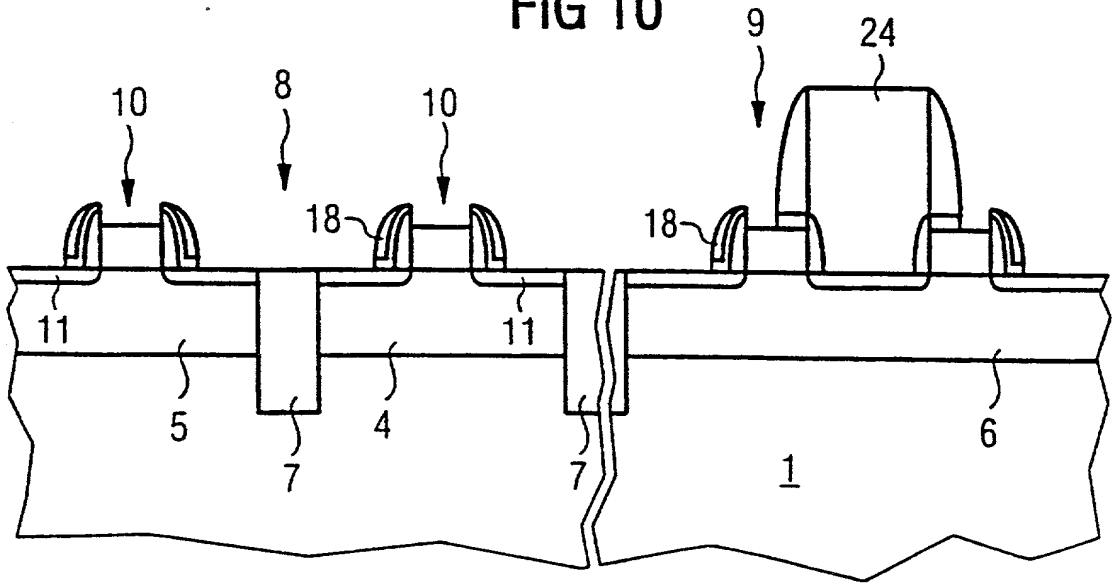

FIG 11

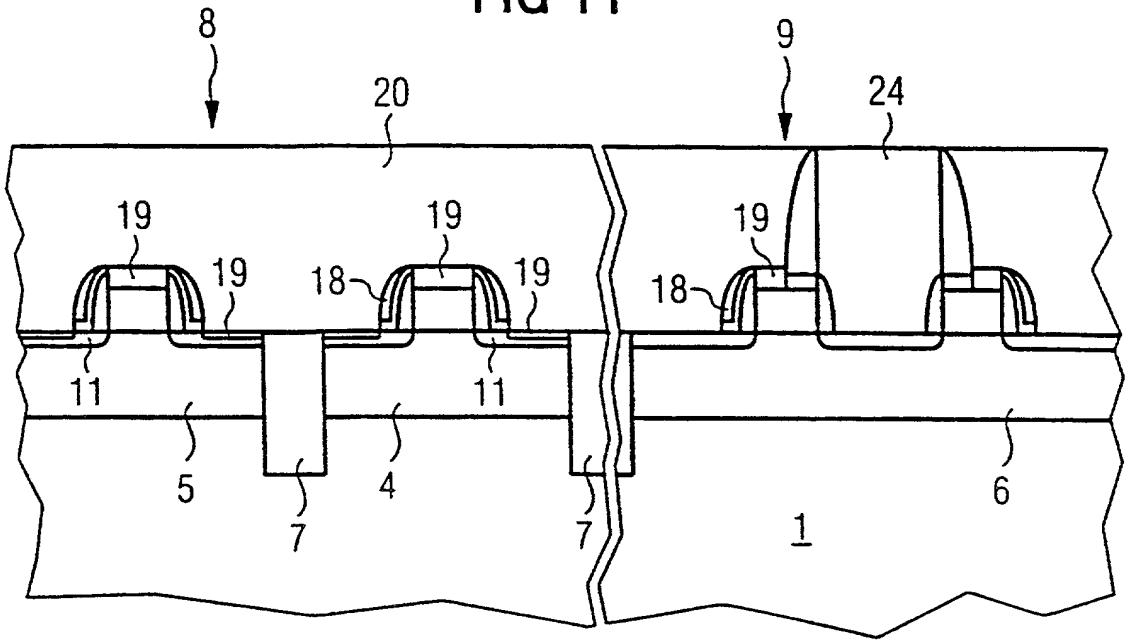
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FIG 12

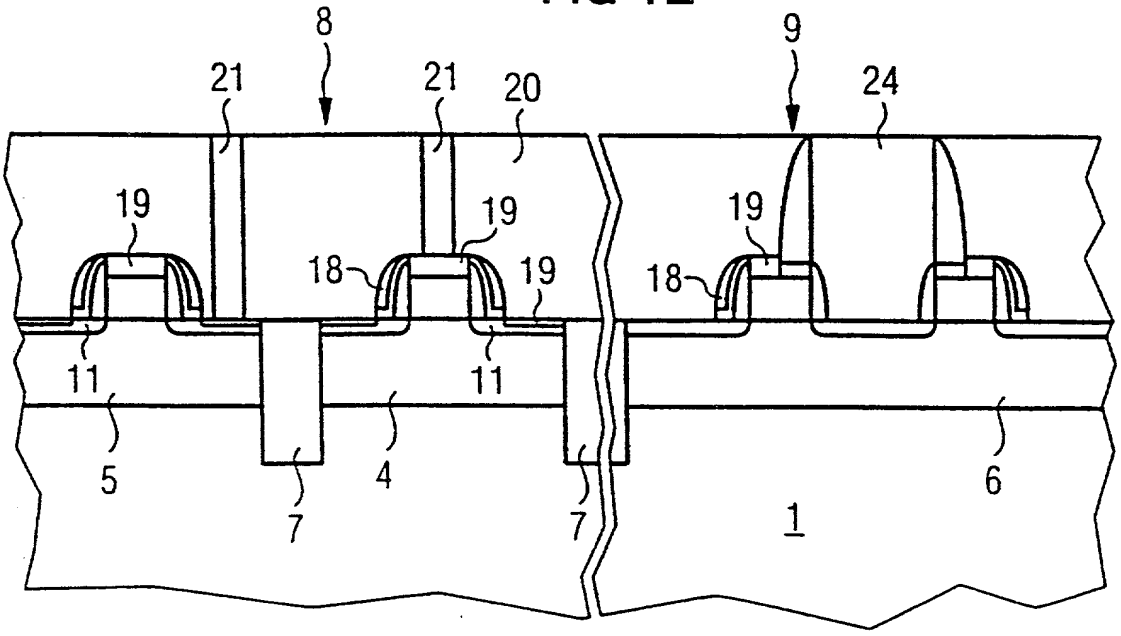
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FIG 13

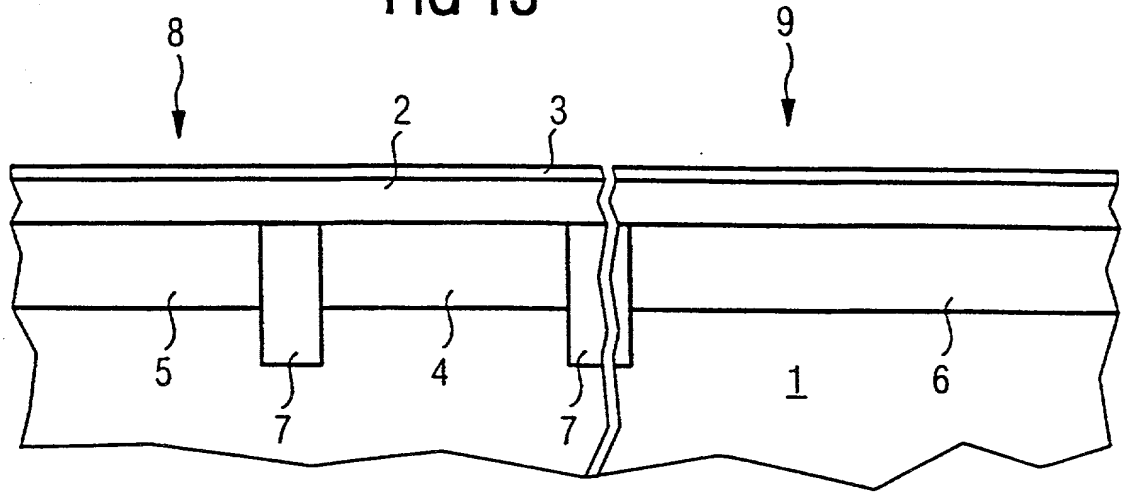

FIG 14

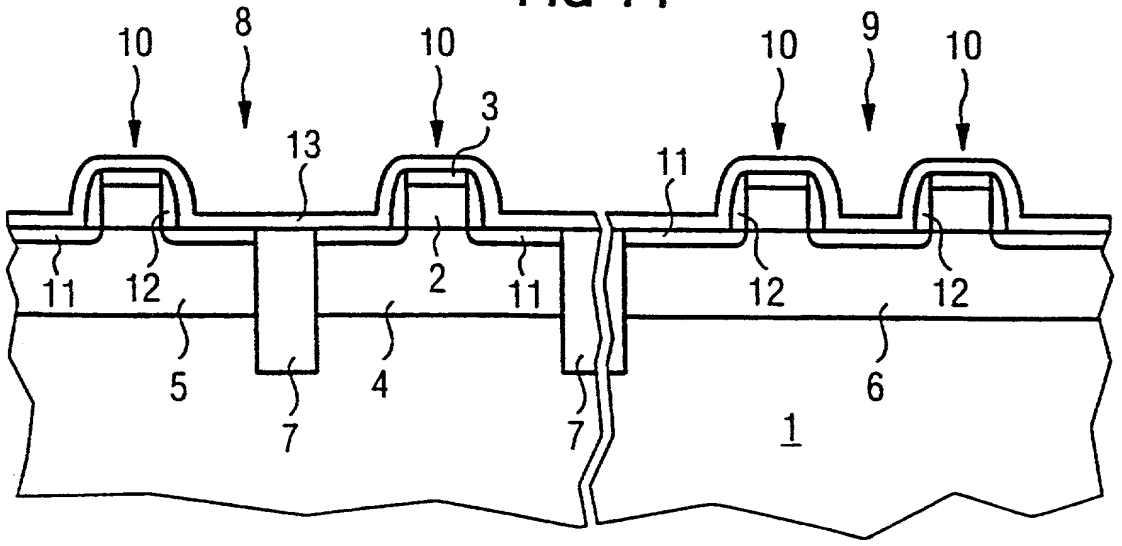

FIG 15

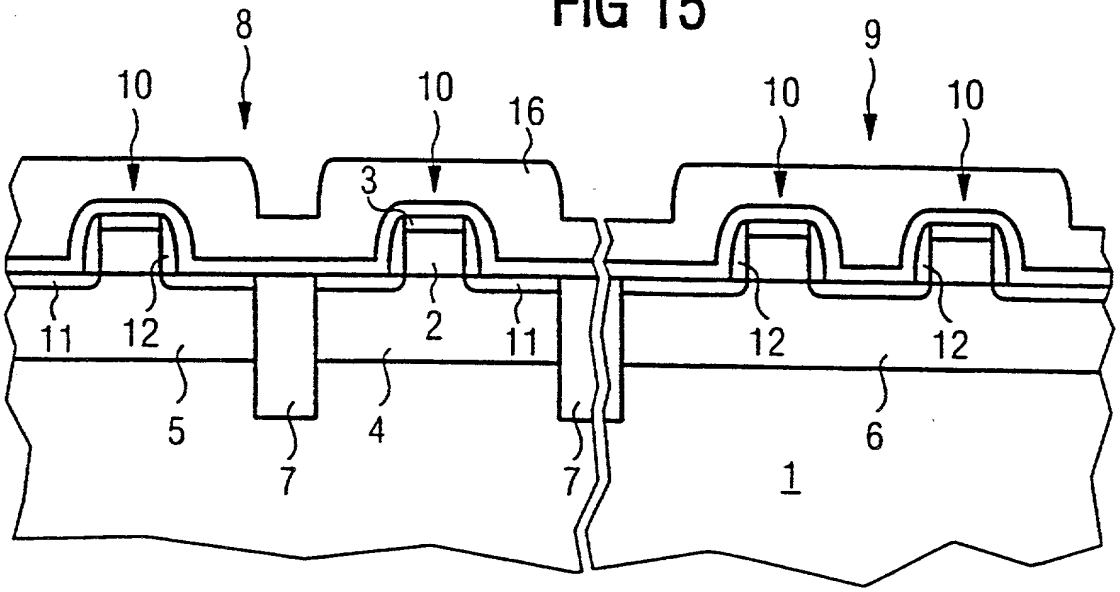
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FIG 16

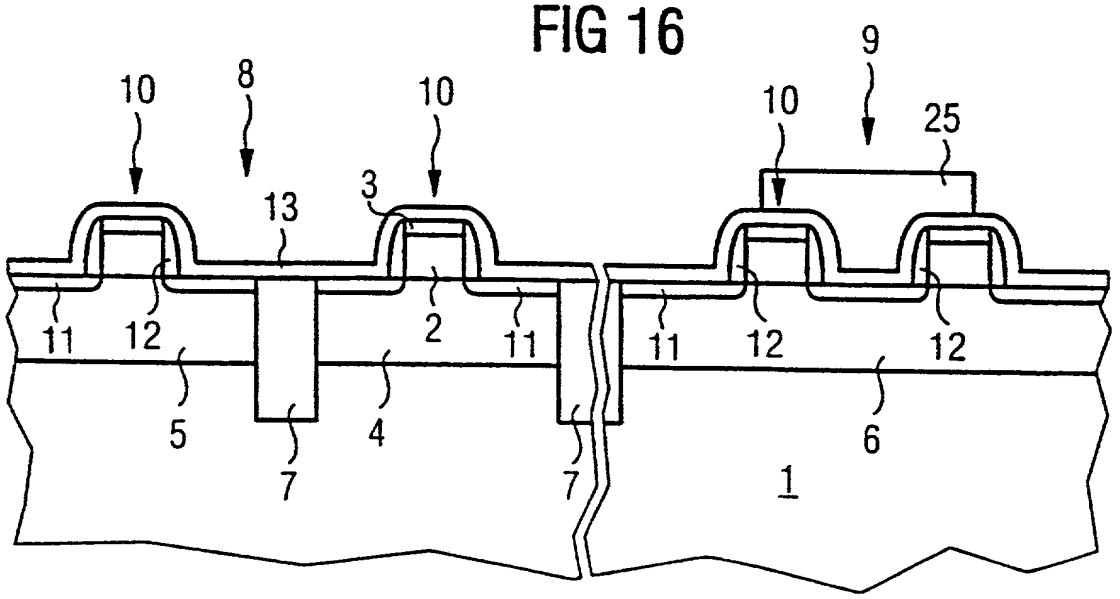
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FIG 17

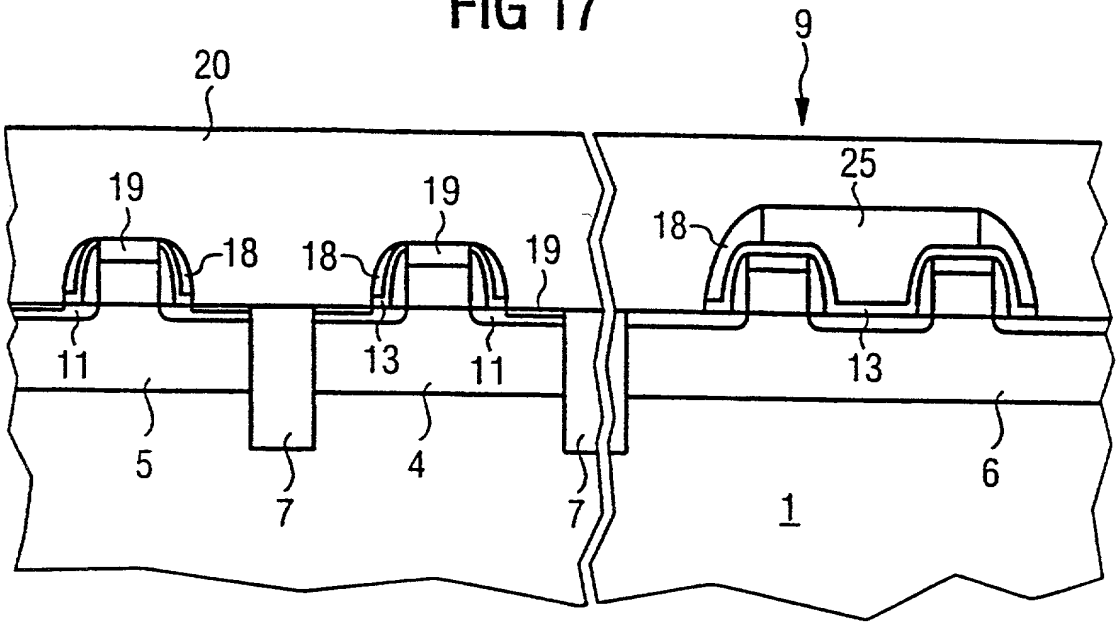
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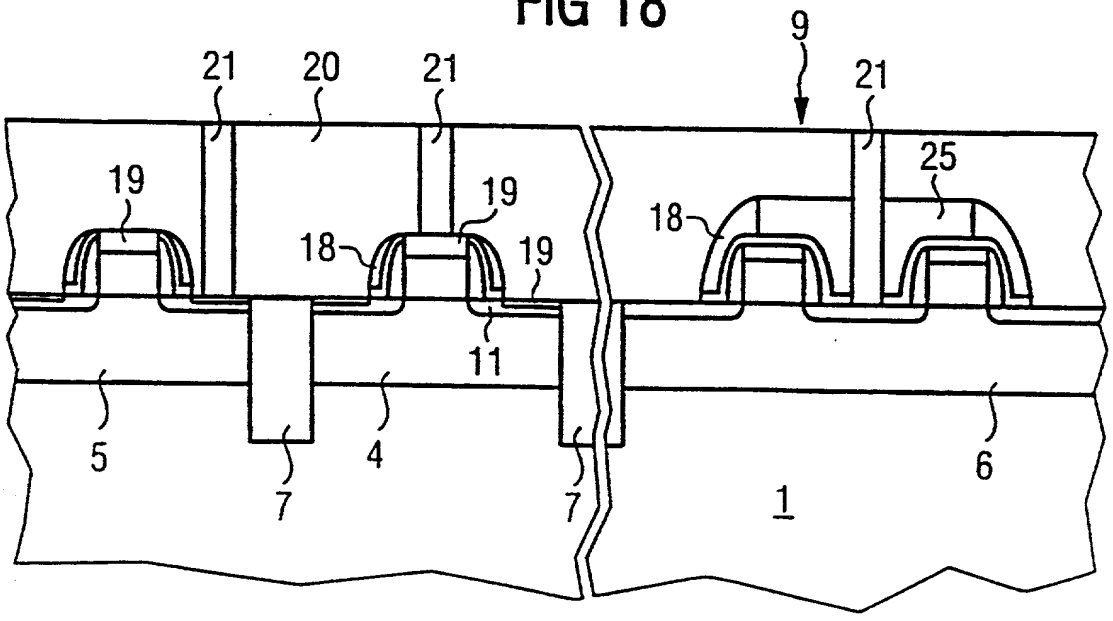
FIG 18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COMBINED DECLARATION FOR PATENT APPLICATION AND POWER OF ATTORNEY
(Includes Reference to PCT International Applications)

ATTORNEY'S DOCKET NUMBER P02,0022

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name, I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

„METHOD FOR PRODUCING INTEGRATED SEMICONDUCTOR COMPONENTS"

the specification of which (check only one item below):

☐ is attached hereto.

☐ was filed as United States application
Serial No. _____

on _____,

and was amended

on _____(if applicable).

☒ was filed as PCT international application

Number PCT/DE99/02339

on 29 July 1999,

and was amended under PCT Article 19

on _____(if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate or of any PCT international application(s) designating at least one country other than the United States of America listed below and have also identified below any foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed:

PRIOR FOREIGN/PCT APPLICATION(S) AND ANY PRIORITY CLAIMS UNDER 35 U.S.C. 119:

COUNTRY (if PCT indicate "PCT")	APPLICATION NUMBER	DATE OF FILING (day, month, year)	PRIORITY CLAIMED UNDER 35 USC 119
PCT	PCT/DE99/02339	29 July 1999	☒ YES ☐ NO
			☐ YES ☐ NO
			☐ YES ☐ NO
			☐ YES ☐ NO

Combined Declaration For Patent Application and Power of Attorney (Continued)
(Includes Reference to PCT International Applications)

ATTORNEY'S DOCKET NO. P02,0022

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) or PCT international application(s) designating the United States of America that is/are listed below and, insofar as the subject mater of each of the claims of this application is not disclosed in that/those prior application(s) in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56 which occurred between the filing date of the prior application(s) and the national or PCT international filing date of this application.

PRIOR U.S. APPLICATIONS OR PCT INTERNATIONAL APPLICATIONS DESIGNATING THE U.S. FOR BENEFIT UNDER 35 U.S.C. 120:

U.S. APPLICATIONS		STATUS (Check one)		
U.S. APPLICATION NUMBER	U.S. FILING DATE	PATENTED	PENDING	ABANDONED

PCT APPLICATIONS DESIGNATING THE U.S.					
PCT APPLICATION NO	PCT FILING DATE	U.S. SERIAL NUMBERS ASSIGNED (if any)			

POWER OF ATTORNEY: As a named inventor, I hereby appoint all Attorneys identified by United States Patent & Trademark Office Customer Number 26574, who are all members of the Firm Schiff Hardin & Waite.

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	RESIDENCE & CITIZENSHIP	CITY: 81929 Munich	STATE OR FOREIGN COUNTRY: Germany	COUNTRY OF CITIZENSHIP: Germany DEX
	POST OFFICE ADDRESS	POST OFFICE ADDRESS: Stefan-George-Ring 47	CITY: 81929 Munich	STATE & ZIP CODE/COUNTRY: Germany

are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

SIGNATURE OF INVENTOR 201	SIGNATURE OF INVENTOR 202	SIGNATURE OF INVENTOR 203
DATE 24-01-2002	DATE	DATE

are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent ~~issuing~~ thereon.

SIGNATURE OF INVENTOR 201	SIGNATURE OF INVENTOR 202	SIGNATURE OF INVENTOR 203
DATE	DATE 22.1.2002	DATE

are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

SIGNATURE OF INVENTOR 201	SIGNATURE OF INVENTOR 202	SIGNATURE OF INVENTOR 203
DATE	DATE	DATE 21.1.02